SLT Circuit Design Handbook

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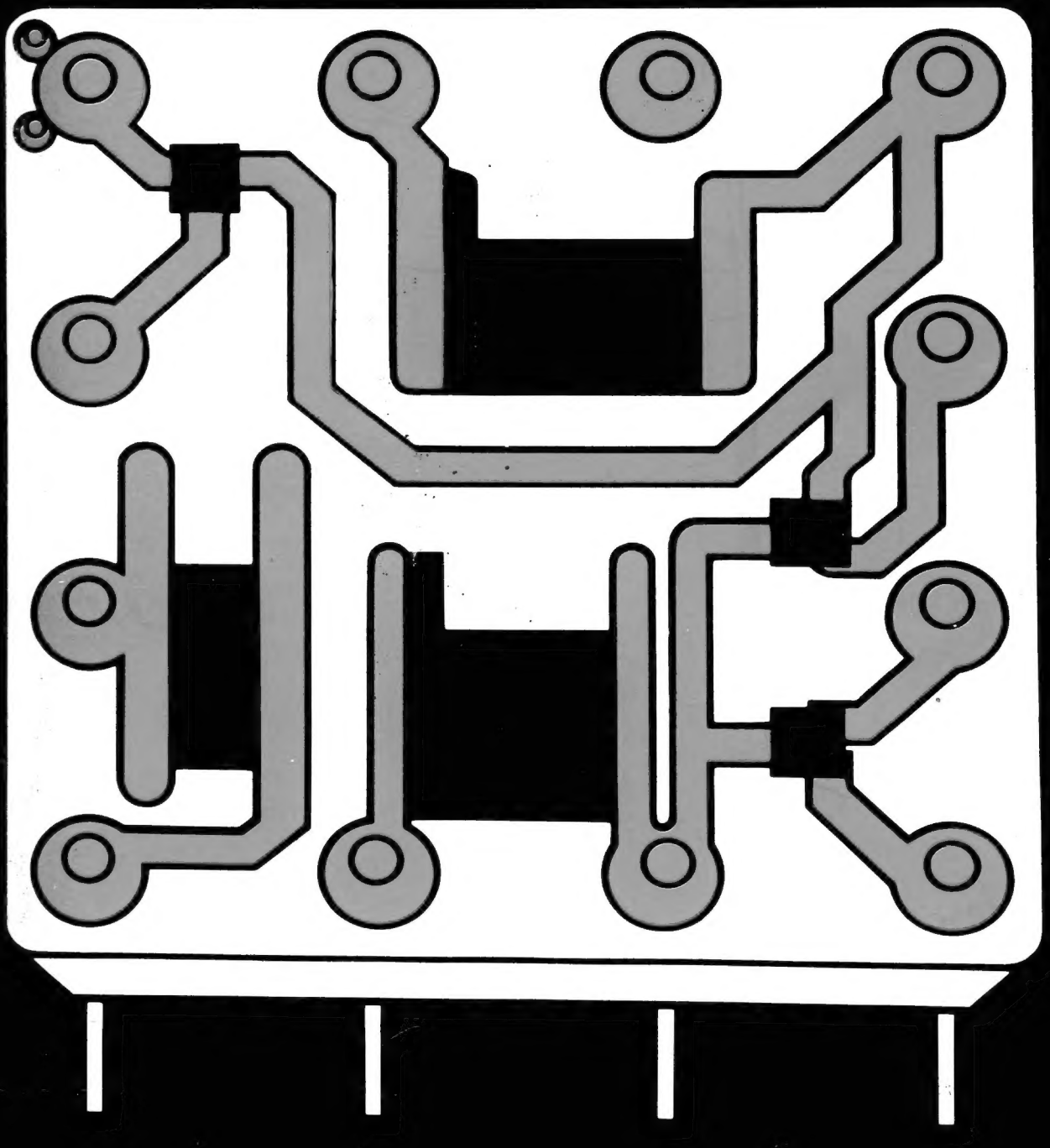

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SLT CIRCUIT DESIGN HANDBOOK

1.0 SOLID LOGIC TECHNOLOGY: VERSATILE, HIGH-PERFORMANCE MICROELECTRONICS.

1.1 Introduction

A new microelectronics technique called Solid Logic Technology, or SLT, is utilized in the family of IBM SYSTEM/360 computers. This technology provides a hybrid, integrated circuit module which combines discrete, glass-encapsulated silicon transistors and diodes with stencil-screened land patterns and precision passive components. The semiconductor devices are fabricated and tested separately, permitting precise parameter control. In the fabrication process these devices are attached to ceramic substrates containing tight-tolerance passive elements. The resultant module is a high-performance, minimum-power circuit in which parasitic interactions are minimized because of the electrical isolation of the discrete components. The design makes feasible hybrid, integrated circuits having close to maximum performance.

The configuration of the semiconductor chip device is the most novel aspect of the technology. The transistors and diodes designed for this approach incorporate a protective encapsulating layer of glass. Contacts from the active regions are brought out through openings in the glass layer to solderable terminations. The semiconductor chips are attached to terminations on the substrate conductor pattern by a solder reflow process. These features permit low fabrication cost and a great flexibility of circuit configurations with minimum trade-off of circuit performance.

2.0 FABRICATION PROCEDURE

2.1 Advantages

The approaches taken in developing SLT were directed toward solving some of the problems generally prevalent in other forms of microelectronics packages. The technology that resulted from the development efforts has shown that hybrid, integrated circuits can be fabricated for high performance and flexibility of application. The processes that are employed in the fabrication of both active and passive components are a major factor in the quality and reliability.

The advantages of this technology can be listed as follows:

a. Graphic arts techniques are used to produce high-quality passive components having tight tolerances.

b. Silicon planar glass-encapsulated transistors and diodes are used. These glassed devices do not require a hermetically sealed enclosure to provide long life and highly reliable performance. A soldering process is used to join these "chip" devices electrically and mechanically into the passive components circuit.

c. The ability to obtain optimized parameter control for the transistors and diodes while simultaneously but independently exercising a tight tolerance control on a wide range of resistors or other passive components permits the attainment of close to maximum circuit performance.

d. A hermetic package is not mandatory.

e. Thermal difficulties are minimized through the use of materials and configurations that have low thermal resistance. In addition, the tight-tolerance circuit components reduce the power required to perform a given circuit function.

f. Parasite interactions are reduced to a minimum.

2.2 Transistor-diode-resistor module

The major features of an SLT module are best understood by reviewing the procedure, step by step, that is used in the fabrication of a typical circuit module, AND OR INVERT (AOI) logic block in the SLT "A" family.

Transistor-diode-resistor module (con't.)

In this AOI circuit, an average logic delay of 20 nsec is characteristic when fan-in and fan-out ratios of 5 are provided. A completed AOI module is shown in Fig. 1a and the circuit diagram in Fig. 1b.

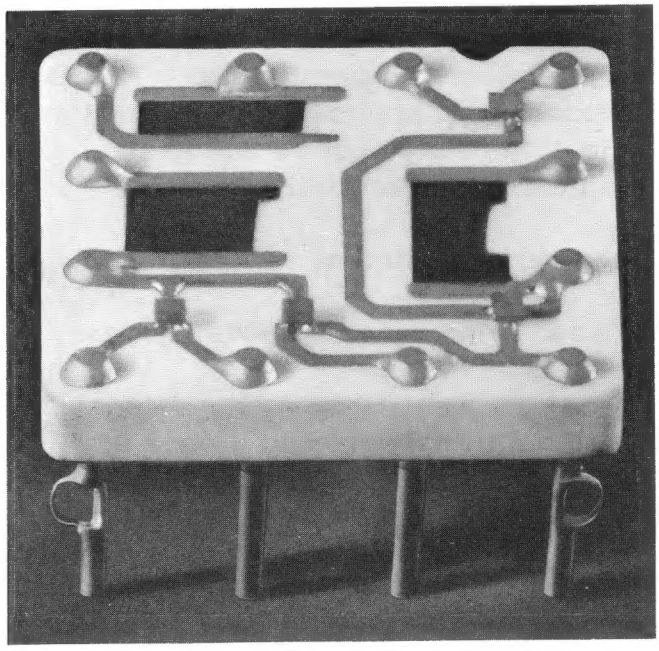
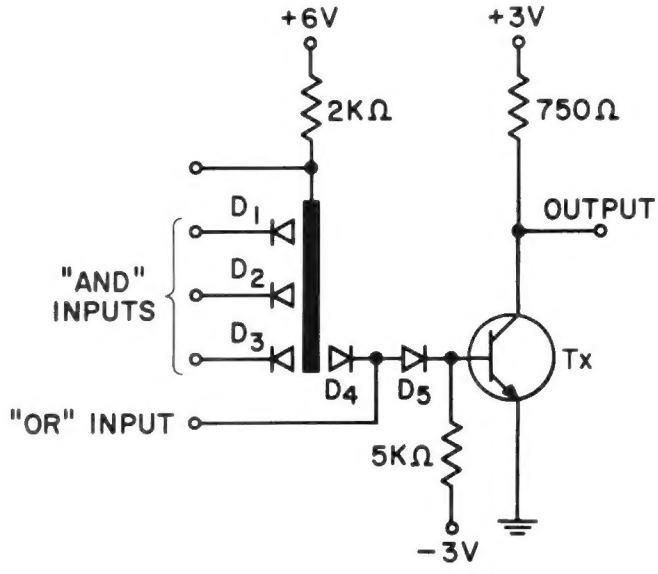


Figure 1:
AND/OR INVERT logic module.
(a) Completed AOI module, without overcoating.
(b) Logic circuit



POWER DISSIPATION : m.w.

	ON	OFF
RESISTORS	28	19
T_X	7	0
D_1, D_2, D_3	0	2
D_4	1	1
D_5	1	1
TOTAL ▶	37	23

ALL RESISTORS: ±5%

The unique configuration of the silicon devices used in the SLT circuits is illustrated in Fig. 2. The chip transistors and diodes are silicon planar glass-encapsulated devices with all external terminals on one surface. Figure 2a is a view of the transistor and Fig. 2b of the diode, showing the side with the external terminals. Dual diodes in single-chip form are used because of their obvious spacesaving advantages over single-chip diodes. Figure 2c shows a sketch, not to scale, of a cross section of the transistor.

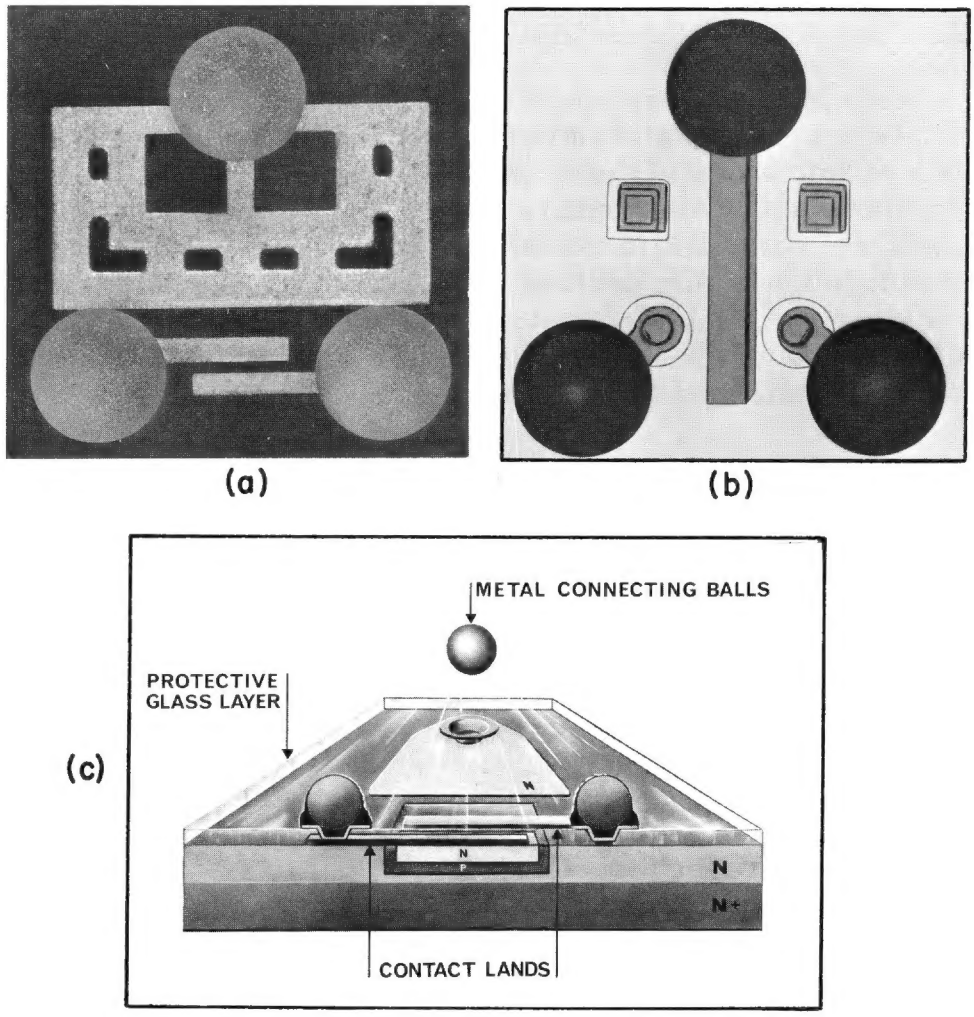


Figure 2: Glassed semiconductor chip devices. (a) Transistor (b) Diode (c) Cross section of Transistor

2.3 Transistor and diode fabrication

As is usually the case for devices of this type, hundreds of transistors or diodes are fabricated simultaneously on a single wafer of silicon. The semiconductor devices are produced using the conventional methods of masking, etching and diffusion. We depart from conventional techniques in fabricating the contacts and terminations. Note from Fig. 2c that contact lands extend away from the small-geometry emitter and base. These lands must be capable of withstanding high temperatures because in the next step the device undergoes a novel glassing operation.

Contacts to the emitter, base, and collector regions are accomplished with solderable metal balls. To attach these balls to the transistor, holes are etched through the glass layer to make available small regions of the emitter, base, and collector land contacts. A metallic layer is evaporated to cover the hole in the glass and extends out on the glass surface. The purpose of this layer is to contact the metal land in the hole and to anchor the metal ball in position by means of an inter-

mediate layer of evaporated solder. We refer to this as the ball-limiting layer. Each wafer is placed beneath a jig so that balls may be placed into holes in the jig for alignment with the ball-limiting layer on the wafer. When heat is applied to the wafer, the solder film fuses, attaching each ball to the wafer. In the final step, each wafer is cut into individual chip devices. On each chip, the ball contacts to each region are available on a single surface. These balls serve ultimately as a means for electrical contact and mechanical attachment when the chips are attached to the substrate.

The transistors are completely tested before being committed to a module. They may be subjected to temperatures in excess of 300°C, during the process of fusing them to the circuit substrate. without appreciable change in their electrical or mechanical properties.

2.4 Passive components

The processes employed to produce the passive components begin with a ceramic substrate, nominally 0.455 "x0.455" x0.060". This substrate contains 12 holes into which pins will later be inserted. A 95% alumina ceramic was chosen because of its good thermal, electrical, and high-temperature properties. The thermal conductivity of the 95% alumina ceramic is approximately 12 BTU/hr/ft/°F, which is about that of stainless steel. The high-temperature ceramic is necessary since most of the critical processes for module fabrication are executed at 300° to 850°C.

The interconnection land pattern is printed on the substrate, as indicated in Fig. 3a. Inks containing noble metals with a glass frit binder are used. Stencil screening techniques are used to print the land pattern, which is then fired onto the substrate at about 850°C. During the firing, the glass frit reacts with the alumina substrate to form an intermediate oxide phase. This oxide serves as a binder between the metallic particles and the alumina. The typical as-screened thickness of conductive lines is 0.5 mil.

The resistors are printed by the same methods as the land materials. The resistor material is a palladium-silver-glass composition dispersed in an organic vehicle. When the screened resistor paste is fired at about 750°C, palladium oxide forms in a matrix of the palladium-silver-glass binder. The palladium oxide controls the electrical properties of the resistor. In addition, the temperature dependence of carrier concentration yields a temperature coefficient of resistance that is a parabolic function of temperature. Changes in resistor composition and screening conditions can produce a resistivity range of 50 to 50,000 ohms per square. The temperature coefficient in the range 25° to 100°C is somewhat dependent on the resistivity of the paste. For example, it is approximately +350 ppm/°C for the 3,000 ohms/square paste, and +200ppm/°C for 5,000 ohms/square paste. These resistors can withstand severe conditions of temperature and humidity with no protective overcoat.

2.5 Pins

In the next step, copper pins approximately 230 mils long and 20 mils in diameter are inserted into the holes in the substrate. Mechanical forces are applied, causing the metal to flow above and below the substrate. Such a pin will withstand, typically, a pull test of 15 lbs. Figure 3b is a general view of a pinned module. The tool that upsets the pins forms them simultaneously to a spacing of 125 ± 1 mils, thus greatly reducing the required tolerance on the holes in the substrate.

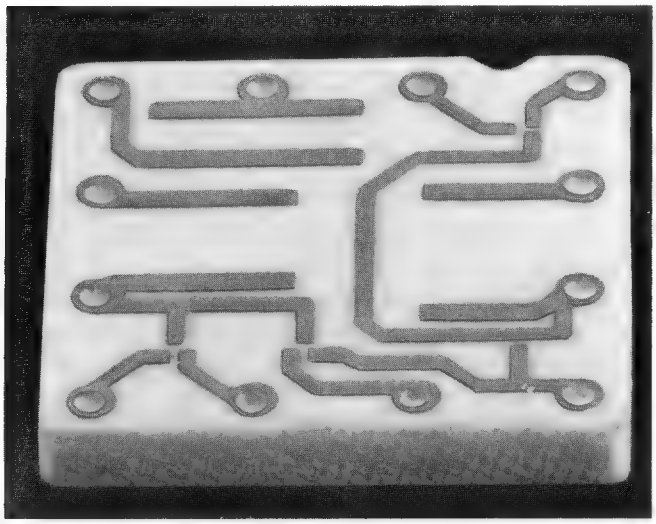


Figure 3a

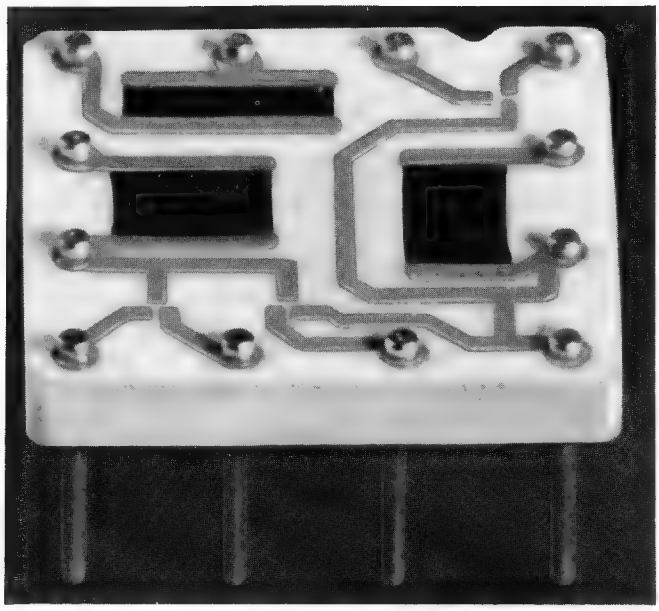


Figure 3b

Figure 3:
Substrate in various stages of processing. (a) With land pattern printed. (b) After pin insertion.

2.6 Solder tinning

The entire module is next immersed in a solder bath at 330°C. Only the lands and pins are wetted by this solder. The solder operation not only insures a good electrical connection between the pins and the lands, but also lowers the series resistance and provides the solder required for joining the land to the semiconductor chip. For example, line widths of 0.005" are reduced in resistance from 20 to 5 ohms/inch, and 0.015" width lines from 7 to 0.6 ohms/inch after they have been tinned.

Uniform solder height across the module is important. This uniformity is particularly important on the chip attachment pads so that a good solder fillet is obtained from the pad to the ball. To assure this even solder height, the topology of the pad is designed with care.

2.7 Resistor trimming

At this point, the ohmic values of the resistors have a typical distribution of $\pm$ 15%. To permit an optimized yield for the desired resistor values, the average of the distributions are set 15% lower than the desired values. The resistors are then tailored to the desired value by abrasive trimming. First the module is inserted into a fixture that has nozzles directed at each resistor. As the module moves under these nozzles, the fine abrasive stream then erodes the resistor, reducing the resistor width and raising the resistance value. Each nozzle is turned off automatically when the desired resistance value is reached. Resistors are designed to have sufficient area, so that even after the theoretical maximum trimming (50%), they remain within a power density limitation of 20 watts per square inch of active resistor material. A trimmed resistor, showing the area eroded by abrasion, is shown in Figure 1a.

2.8 Joining chips to substrate

After the passive components on the substrate are tested, the semiconductor chips are joined to the approprate attachments pads on the substrate. After the pads are fluxed, the chip devices are positioned and gently pushed into the solder layer on the chip attachment pad. The flux and the cold flow of the solder serve to hold the chips in position during subsequent handling until the solder is reflowed. When heat is applied to the module, the solder melts or reflows and wets the balls on the semiconductor chip to create solder fillets at each ball. The chip has now been electrically and mechanically joined to the substrate. All chips are joined to the substrate simultaneously.

2.9 Encapsulation Assembly

An approach where passivation and "hermetic sealing" are carried out at the device level has considerable merit. If one can be assured that the active portions of the devices have been passivated and can be considered equivalent to hermetic areas, the remainder of the microcircuit can be treated as closely spaced wiring on an interconnection board. In this way, the circuit package can be made non-hermetic in the same manner as the remaining levels of printed circuit wiring.

A typical microcircuit package design has many requirements; however, the major ones for this discussion are created by the necessity to use materials other than inert atmospheres (as in hermetic seals) in contact with the component surfaces. When one considers switching from hermetic to non-hermetic sealing, the plan generally involves changing from a hollow shell filled with an inert gas to an embedment system with plastic materials applied directly to the component. Non-hermetic shells without dielectric materials applied to the component surface would suffer in moisture resistance. Embedding delicate component surfaces and interconnections in a non-hermetic package imposes a few special requirements if high reliability is to be maintained.

These special requirements can be stated as follows:

. A rugged exterior mechanical structure capable of withstanding normal testing, marking, handling, and assembly into the next level package must be provided.

. The structure must minimize the transmission of mechanical stresses caused by thermal expansion mismatching on sensitive interior components.

. The structure must minimize the transmission of mechanical stresses caused by external mechanical shock to sensitive interior components.

. The materials chosen must be chemically stable and maintain a high insulation resistance at elevated temperatures.

. The materials chosen must provide moisture environmental protection over a broad range of temperature and humidity combinations.

It should be apparent that the design philosophy in this case is based on the premise that internal interconnections are more reliable when properly designed and surrounded by non-stressing fluids, rather than being potted or cemented down with rigid materials. These design requirements would be difficult to acheive with a single material and application process, such as molding. A three part-design developed to fulfill these requirements are:

Encapsulation Assembly (con't.)

a.) A silicone dielectric gel conformal coating was used to provide chemical stability and good strength while providing a mechanically stress-free environment for the mounted semiconductors. This material is physically and chemically stable over a range of -50° to 200°C. Its cured hardness can be reproducibly controlled to be an extremely soft (almost fluid) resin which does not flow in the application described.

b.) A hard shell cover was used to provide rugged external structure for handling purposes. Many different metals or plastics would suffice for this purpose. A stamped aluminum cap was chosen.

c.) Attachment of the shell imposes material requirements similar to those of the conformal coating, with the exception of the mechanical characteristics. A silicone rubber adhesive was chosen for this purpose. In addition to supplying a means of attachment for the outer shell, the silicone rubber provides an additional protective seal from the environment. A section drawing indicating design features is shown in Figure 3c.

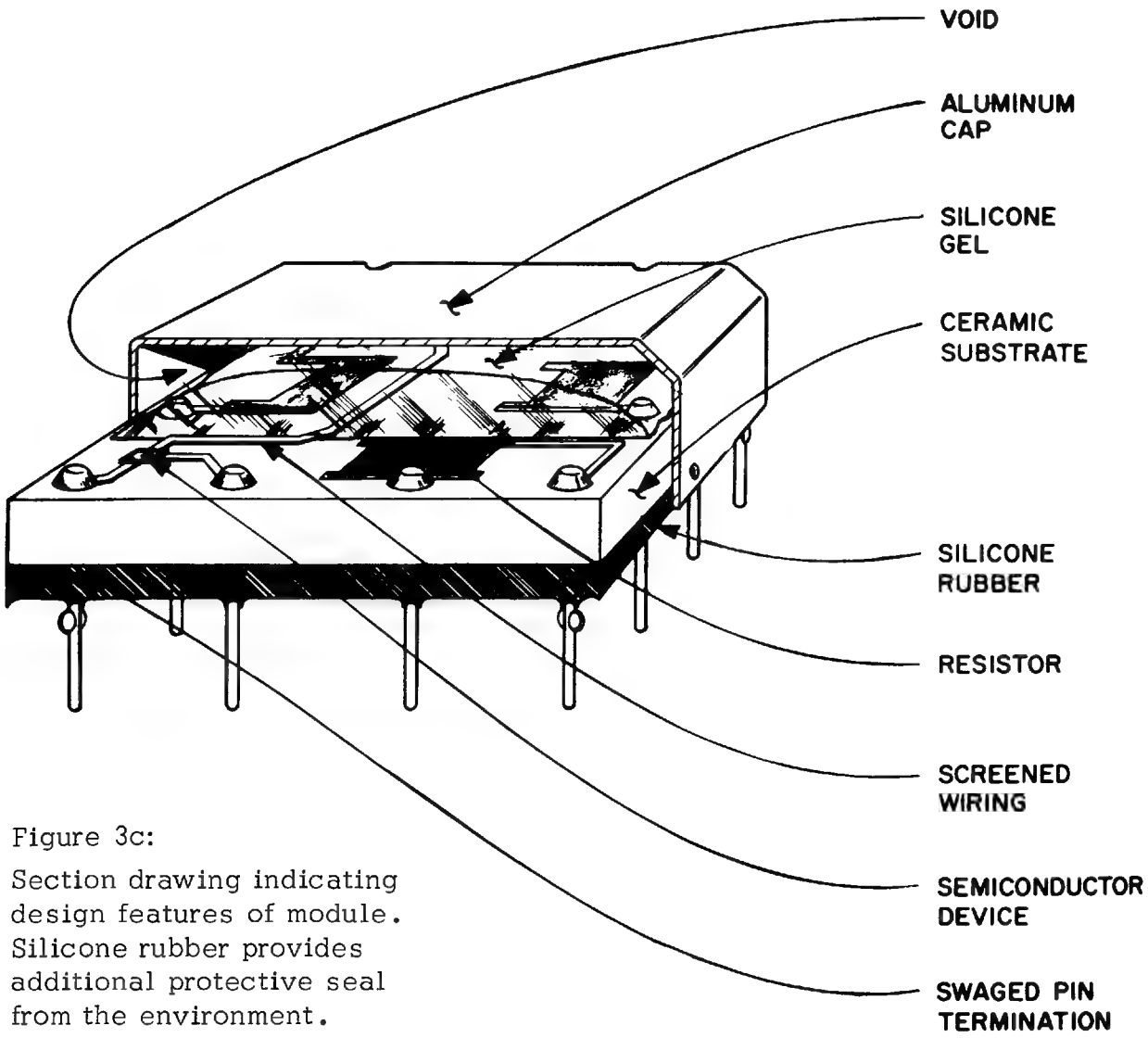


Figure 3c:
Section drawing indicating design features of module. Silicone rubber provides additional protective seal from the environment.

Encapsulation Assembly (con't.)

An important consideration in designing any component package is compatibility with subsequent levels of packaging assembly. Orientation of the module is provided by the bevel on the cap. To permit automatic insertion, tight tolerances must be kept for pin straightness and pin location with respect to the cap. A crimped standoff on the pin provides a uniform space for solvent cleaning after card assembly. The package must be capable of withstanding all assembly handling stresses, thermal exposure of a wavesoldering operation, and chemical exposure of fluxing and solvent cleaning. The RTV-sealed package described meets every requirement readily, including solvent resistance.

The encapsulation assembly is achieved in five basic steps. The materials are mixed in a conventional manner; however, since significant cure times are involved, an accelerated "pre-cure" sample is run to verify that the batches have been properly formulated.

a.) Application of Silicone Resin Gel. The material is dispensed at room temperature onto heated substrates. The substrate temperature (150°C) partially cures the driplet of material as it spreads, preventing runover at the edges. Subsequent heating for 20 min at 160°C completes the cure. Substrate temperature, shot size, and location must be reasonably well controlled to avoid silicone coating of the edges.

b.) Capping. The conformal-coated module is inserted into the aluminum cap. The cap has four stand-off ridges formed during stamping to support the substrate in its final position. After insertion, a small dimple is punched into the can on four sides to secure the substrate and maintain alignment during further handling. The cap has one beveled edge which serves as an alignment feature for automatic machine handling.

c.) Primer Application. A primer to enhance the adhesion of the silicone rubber backseal is dispensed. The material is carried in an acetone diluent which evaporates quickly leaving a thin uniform film. The film is permitted to dry and cure for 1 hr. at room temperature.

d.) Backseal Potting. The Room-Temperature-Vulcanizing silicone rubber mixture is diluted with toluene to provide a viscosity of approximately 500 centipoises. Viscosity control for good coverage without seepage and bubbles is fairly critical. A quantity sufficient to give complete filleting at the edge is dispensed. The minimum RTV thickness required at the seal area is approximately 0.030 in.

e.) Backseal Cure. To achieve good adherence and strength in the seal, the RTV cure must be carried out under controlled temperature and humidity conditions. The material is cured at room temperature for 4 hrs. to permit evaporation of the toluene and initial curing of the rubber. The humidity should be controlled between 50% to 70% rh for RTV using a hydrolysis type curing mechanism. Having achieved a firm cure, the parts are next elevated gradually to 170°C and held for 2 hours.

2.10 Some test results

The resistors and semiconductor devices have been exposed to severe environmental stress conditions for long periods of time to determine stability under non-hermetically sealed conditions. Figure 4 shows 5,000-and 10,000-hour data on resistor drift under various stress conditions.

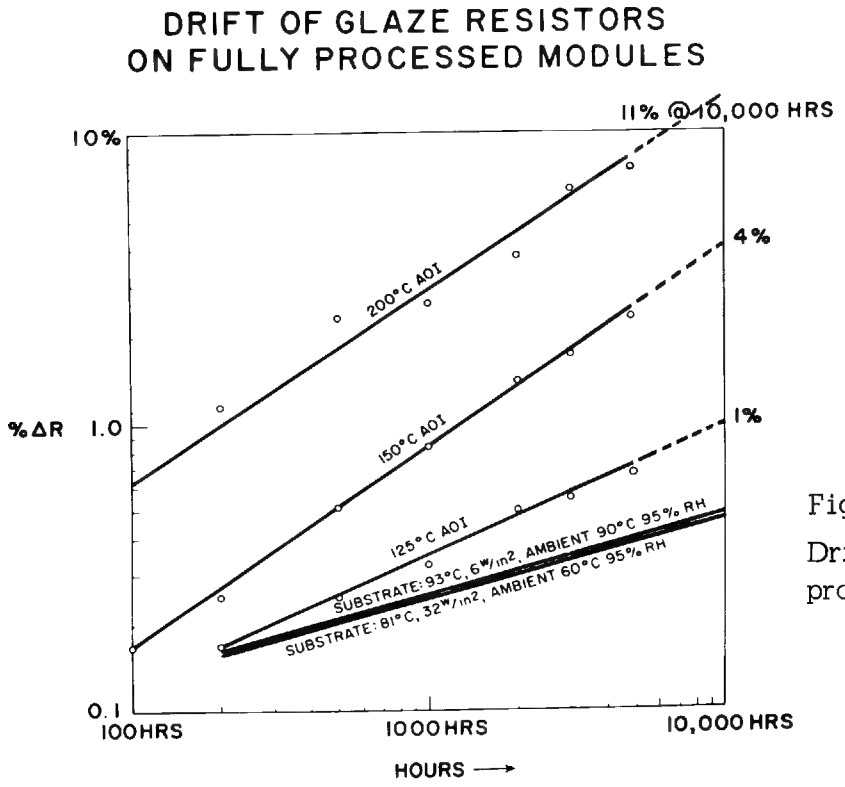


Figure 4:
Drift of glaze resistors on full processed modules.

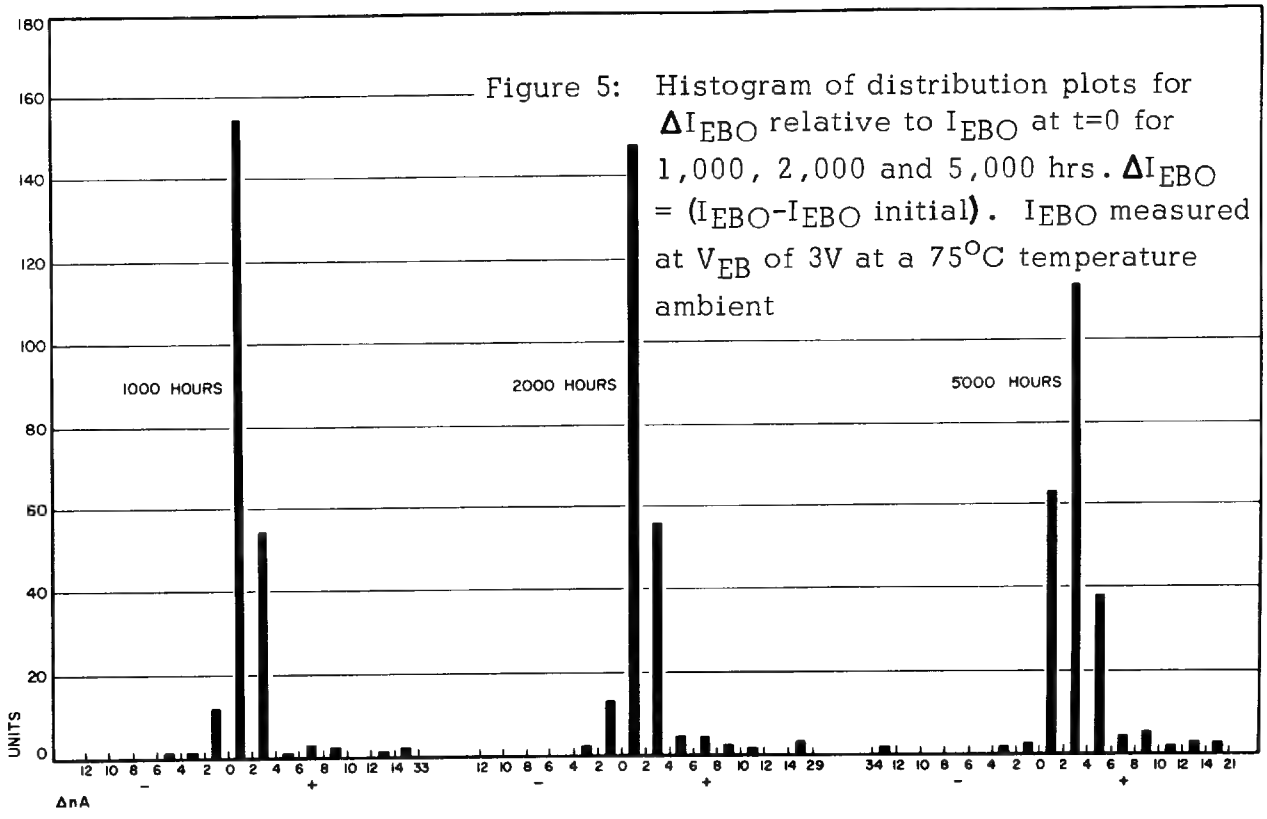


Figure 5: Histogram of distribution plots for ΔI_{EBO} relative to I_{EBO} at t=0 for 1,000, 2,000 and 5,000 hrs. ΔI_{EBO} = (I_{EBO}-I_{EBO} initial). I_{EBO} measured at V_{EB} of 3V at a 75°C temperature ambient

Some test results (con't)

Note that resistance increased with time, although slight negative drifts do occur during the first 200 hours. Drift in these resistors is largely a function of temperature, and the resistors are generally insensitive to humidity or power fluctuations. The data shown are for medium-resistivity materials (500 to 3,000 ohms/square).

Figures 5 and 6 indicate parameter behavior, measured at 75°C, after testing 236 transistors for 5,000 hours. One group of these devices (48 transistors) has been maintained in an 85°C ambient and power pulsed (150 mW) so that the junction temperature cycled between 85°C and 150°C. A second group (89 transistors) has been stored at 150°C with V_{ce}=8V and V_{be}=-4V, and the third group had been stored at 85°C, 85% RH with V_{ce} = 8V and V_{be} = -4V.

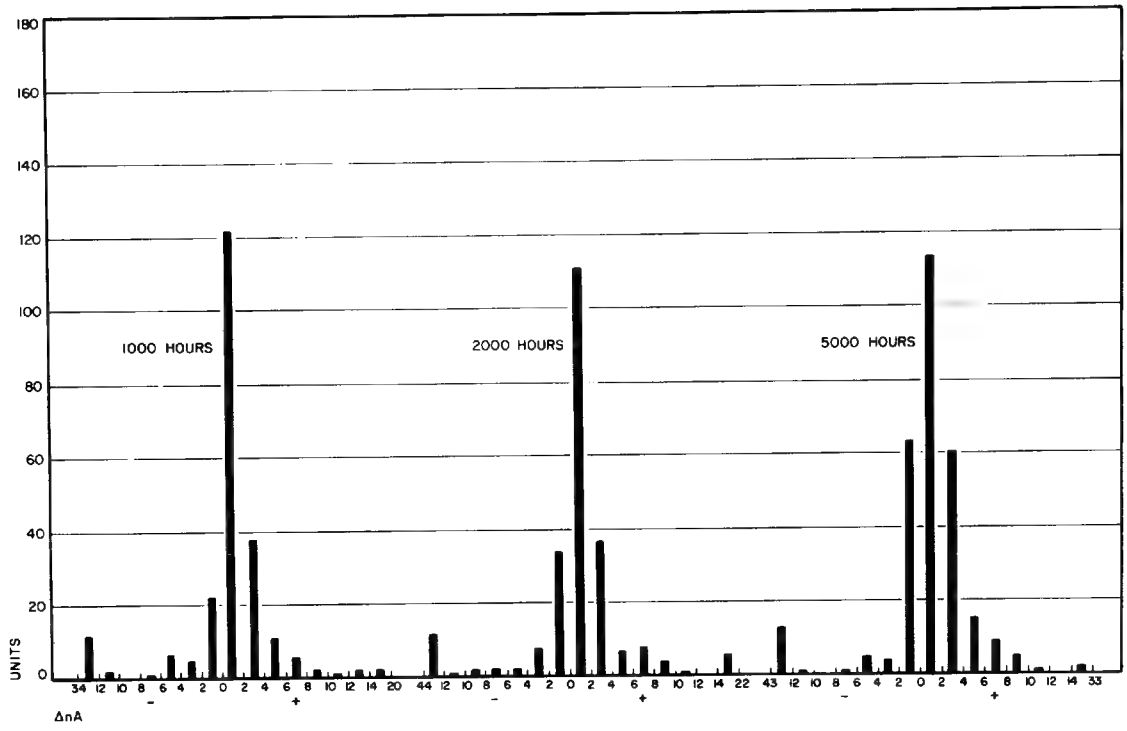


Figure 6: Histogram of distribution plots for ΔI_{CBO} relative to I_{CBO} at t=0 for 1,000, 2,000 and 5,000 hrs. $\Delta I_{CBO}=(I_{CBO}-I_{CBO\ initial})$. I_{CBO} measured at V_{CB} of 6V at a 75°C temperature ambient.

The intent of this test was to examine the stability of the glass-encapsulated semiconductor junctions. The stability of the data gathered indicates that there are no processes occurring that deteriorate junction properties. Other device parameters, such as junction breakdown voltage, current gain, and the forward characteristics of the junctions, were measured and show similar stability. Three transistors in the 150°C group were removed from this distribution because of gross deviations not related to junction failure mechanisms.

2.11 Thermal considerations

As is well known, thermal considerations are of prime importance in microelectronics. Figure 7 shows a plot of the thermal resistance (R_e) of the AOI module and of transistor junction temperature as a function of the air velocity over the module in a typical machine environment. The alumina substrate is essentially an isothermal surface because of its excellent thermal conductivity. The thermal properties of a module then are predicted by the thermal resistance between the chip and the substrate, and the thermal resistance between the substrate and the air. The thermal resistance between the substrate and a transistor junction is typically 0.13°C/mW and has a worst-case value of 0.15°C/mW. The thermal resistance between the substrate and the surrounding air is a function of air velocity. Note that the rise of junction temperature above ambient tends to be small. The circuit designs have been based on a maximum semiconductor junction temperature of 75°C under worst-case environments.

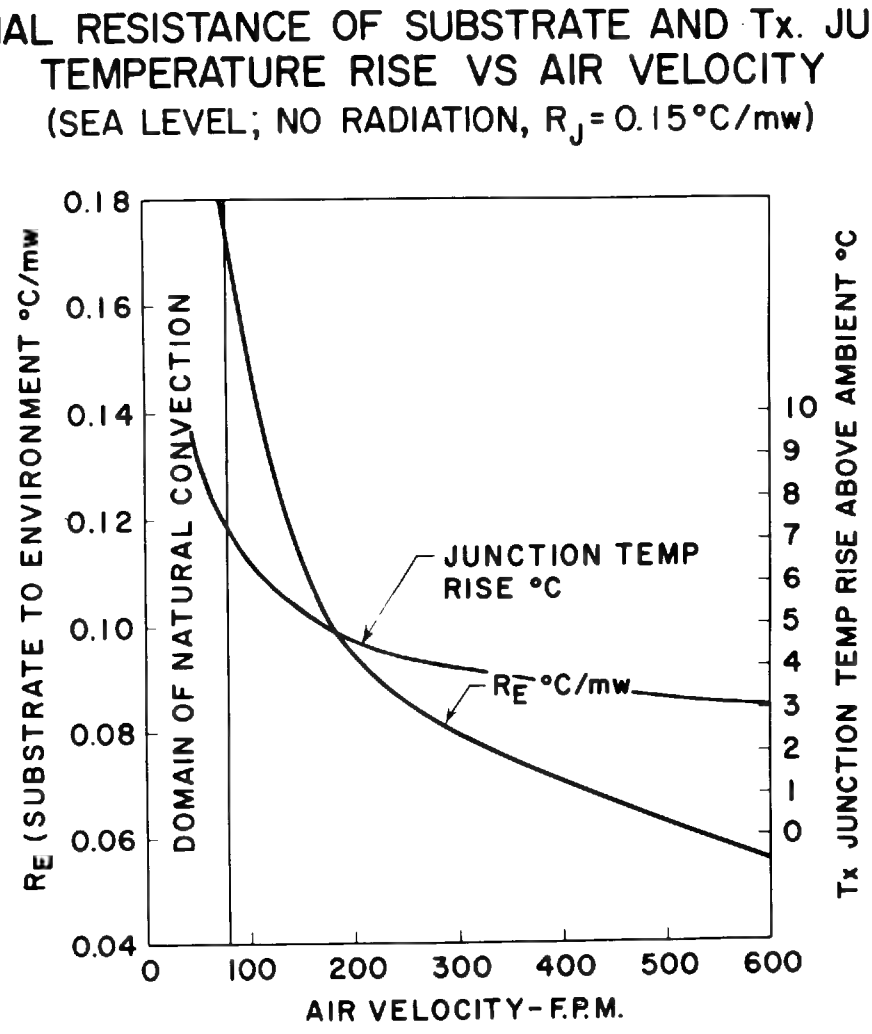


Figure 7: Thermal resistance of substrate and transistor junction temperature rise vs air velocity.

2.12 Reliability Testing

The high-stress conditions generally used by IBM for accelerated testing are 85°C-85% relative humidity. Tests are performed with all semiconductor junctions back-biased. These conditions are intended to provide high voltage stresses simultaneously with high humidity and high temperature. At 85°C-85% relative humidity, a failure rate of 0.28% per 1,000 hr, based on 16.6 million device hr has been recorded. No functional resistor fails have been seen in 21 million device hours of testing. A module field failure rate of less than 0.005% per 1,000 hr has been observed based on 1.5 billion module hr of experience.

2.13 Radiation Doses

SLT modules have been subjected to integrated gamma radiation doses of 10^8 rads. No significant changes occurred in the passive components. More startling, however, is the indication that the glass-over-oxide structure, described earlier, significantly reduces the degradation of transistor leakage (and diode reverse currents) in devices subjected to simultaneous reverse bias and ionizing radiation. It is believed that this reduction of degradation results from the isolation, by the glass layer, of the junction from ions generated in the surrounding gas. These ions are thought to cause the increase of junction leakage currents by collecting on the device surface to form an inversion layer. Diffused silicon diodes and transistors in hermetically sealed headers, with oxide passivation only, were also included in this test as controls.

3.0 SLT CIRCUIT FAMILIES

The basic SLT circuit is the AND-OR-Inverter (AOI).
Circuit speeds are: 700ns & 30ns
Voltage levels are: 0.0v to +3, +12v.
Logic may be diode, transistor, or a combination.
A logic block may use different circuits for each of the two speeds.

3.1 Circuit Speeds

Presently there are two circuit speeds, depending upon the semiconductor (diode and/or transistor) and its switching speed. Switching speeds are in the order of 30, and 700 nanoseconds for each logical block.

3.2 Circuit Voltages

Approximate voltage levels for each of the two speeds of circuits are:

30ns circuit: +0.0v, most negative; +3.0v, most positive.
700ns circuit: +0.0v, most negative; +12.0v, most positive.

3.3 Transitions

Transitions (Figure 1A) is the time a transistor output takes to switch from one logic state to the other. The voltage levels at which the transitions are measured for the different families are:

FAMILY	TRANSITION POINTS
30ns, medium speed	+0.3v & 1.8v
700ns, low speed	+0.29 & 2.0v

Switching times include turn-on transition, turn-off transition, turn-on delay, and turn-off delay. These values are basically the same for each of the circuit families. The major difference is that the transition points and voltage levels vary for each family.

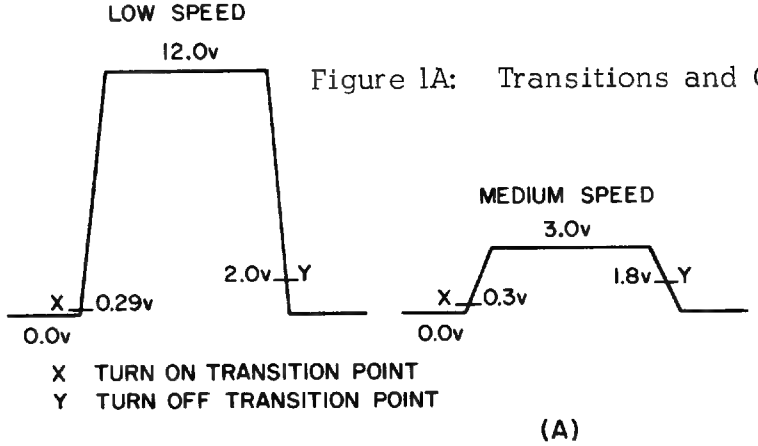
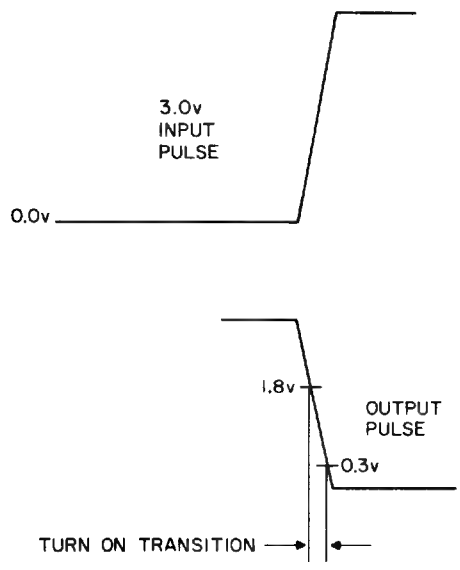


Figure 1A: Transitions and Circuit Measurements.

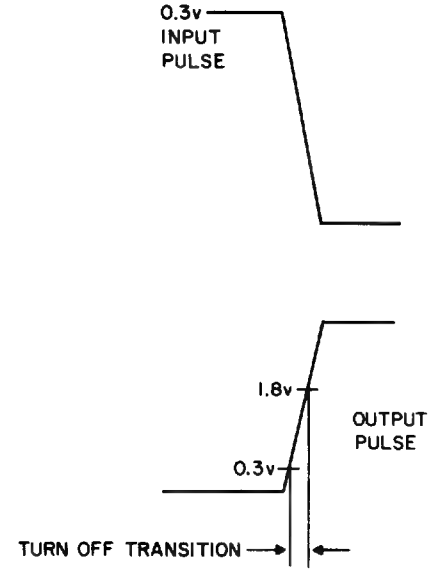
(A)

Turn-on transition (Figure 1b) is the switching time from an off state to an on state. Turn-on transition is measured on the output wave form from a specified value in the nonconducting state to a specified value in a conducting state.

Turn-off transition (Figure 1c) is the switching time from an on state to an off state. Turn-off transition is measured on the output waveform from a specified value in the conducting state to a specified value in a nonconducting state.

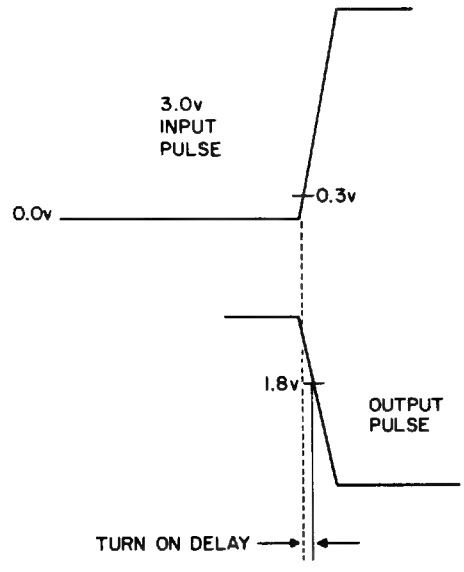


(B)

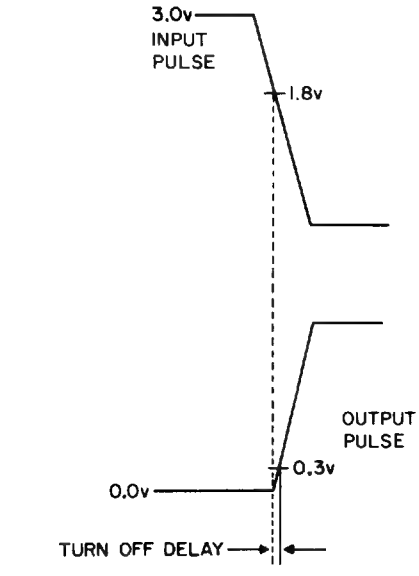


(C)

Turn-on delay (Figure 1d) or turn-off delay (Figure 1e) is the time the circuit takes to change its output state due to a change in the state of input. Switching time is measured from a point where the input wave form has reached a specified value to a point where the output waveform has reached a specified value.

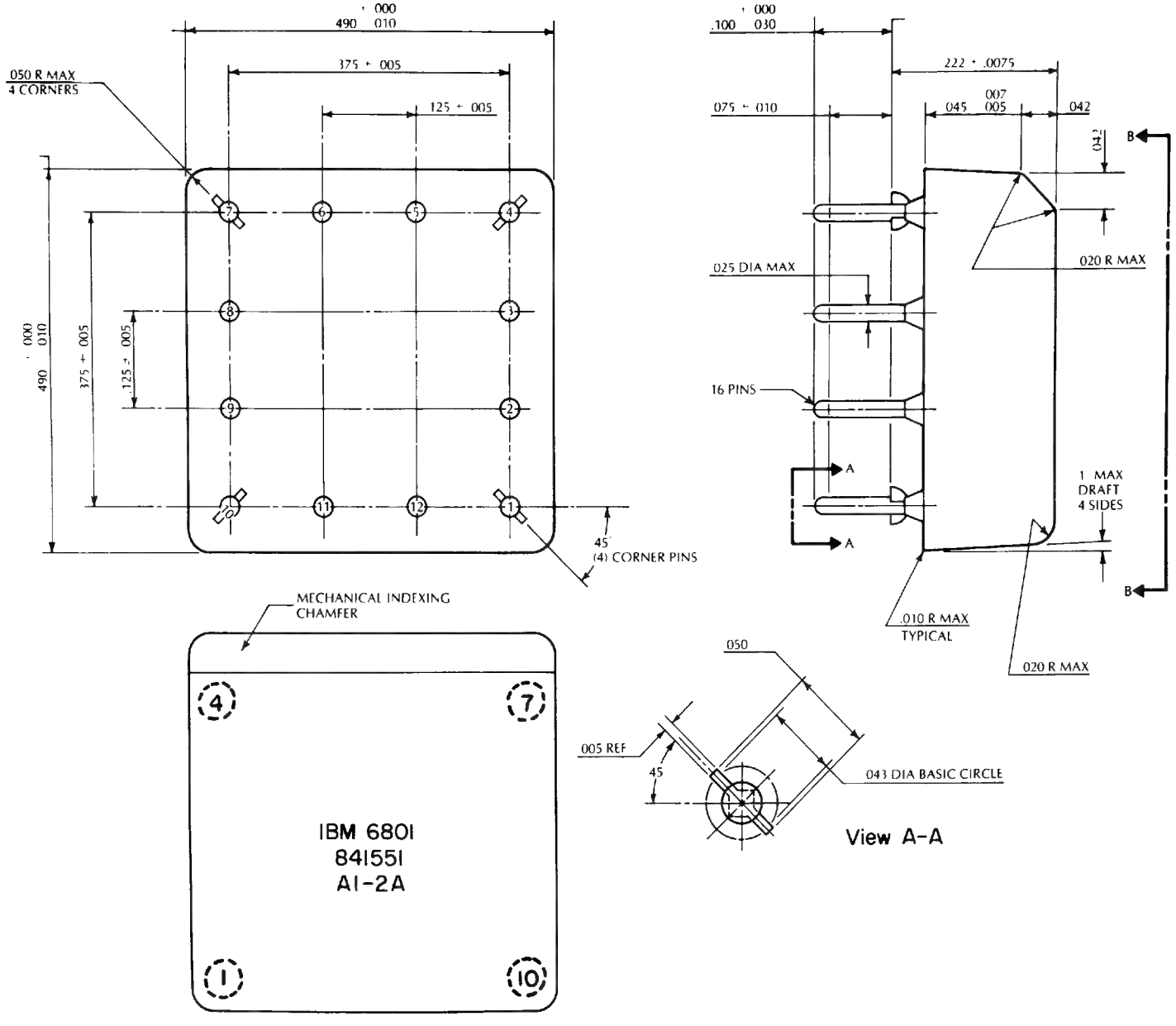


(D)



(E)

4.0 SLT MODULE OUTLINE AND DIMENSIONS



5.0 DESIGNING WITH SLT

5.1 Introduction

The purpose of this section is to illustrate some of the general logic applications and advantages of using SLT technology. A basic design philosophy which has been engineered into the SLT technology is flexibility. This characteristic allows the designer to optimize his design according to his particular needs with a minimum number of components.

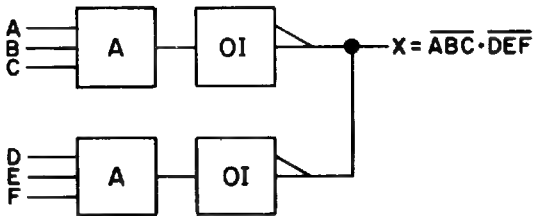
An understanding of the potential offered by each module may be necessary before efficient design is realized. This section will illustrate, with some examples, a few design possibilities. It is important for the logic designer to be sure he does not exceed the circuit specification.

5.2 Dotting and Extending Operations

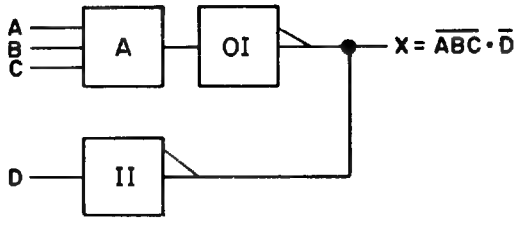
Dotting and extending are two very useful and powerful logic operations. Both of these operations are available to the designer in the SLT technology. The extending operation allows an increase in both the AND fan-in as well as the OR fan-in by the addition of passive components, whereas collector dotting will generate an "OR" function. Examples of these operations are shown below.

5.2.1. Collector Dotting

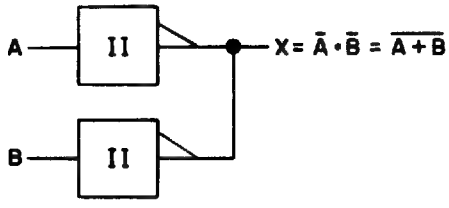
Collector dotting ("dot-OR") performs an OR function with two modules when the transistor collectors are parallel connected with only one collector resistor.



Two AOI's dotted together



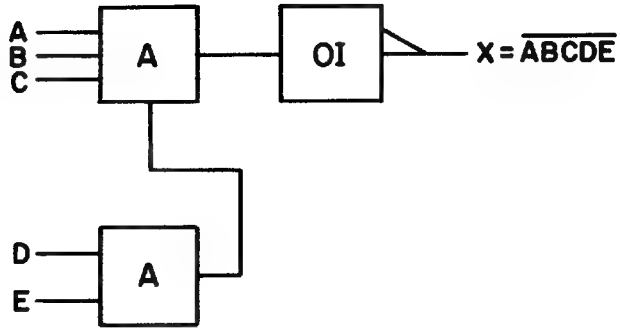
An AOI and II dotted together



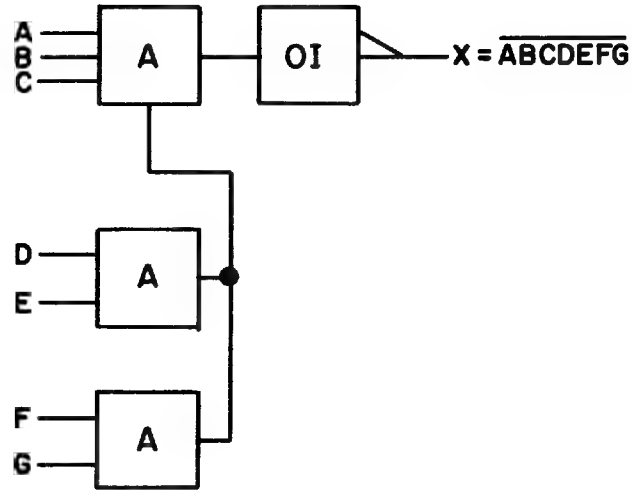
Two II's dotted together

5.2.2. AND-Extend

The AND-extend operation is achieved by combining an FDD with an AOI module, thereby expanding the gate fan-in.



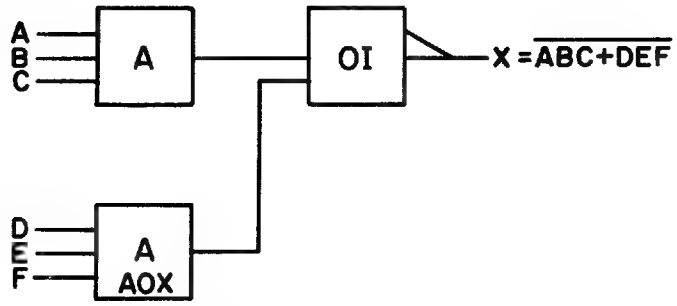
An AOI extended with 1/4 FDD



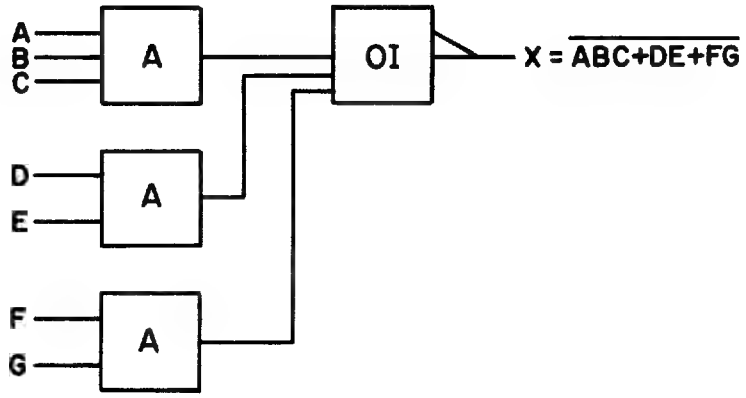
An AOI extended with 1/2 FDD

5.2.3. OR-Extend

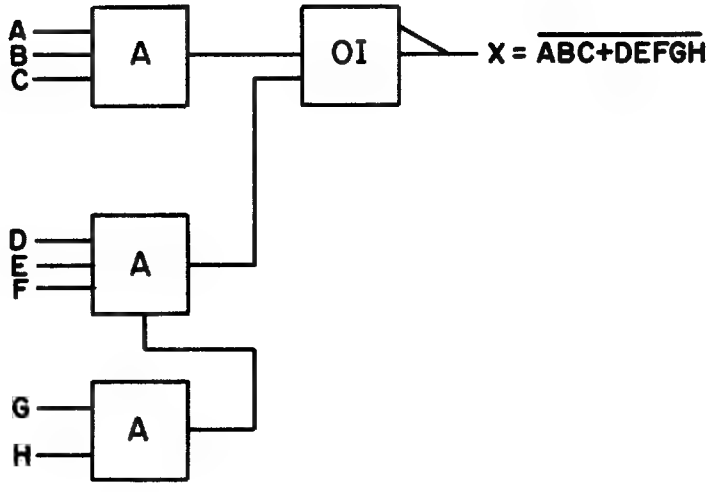
The extent to which the dotting and extending operation can be used is specified for each module type in the circuit specifications.



AOI extended with 1 AOX



AOI extended with 2 AOX



AND-extend OR-extend combination
using an AOI, an AOX, and a FDD.

5.2.4. Hazards

The reliability of a logic circuit is indicated by showing its significant hazards. A hazard signifies that a circuit can malfunction under certain conditions. However, as long as these conditions are not met, the circuit will operate properly. Proper circuit operation is based on the assumption that there is more or less delay in one signal path than in another signal path. Because of the wide range between worst and best case delays, conditions may occur where this assumption proves invalid. Another type of hazard results from the assumption that all blocks react to an input signal change at the same time. Contrary to this assumption, it may be possible for one block to react to an input change and actually have its output change before another block even senses the original input change.

In most cases, a hazardous situation may result in a false positive or negative pulse within the circuit. If the pulse is short, it may not affect the circuit operation, but if the pulse is long enough, it may alter the state of a feedback loop and thus cause the circuit to malfunction.

5.3 Set-Reset Latch

The set-reset latch is a basic two-state memory element capable of storing a single bit of information. There are a number of possibilities in SLT to achieve this function. Two examples are shown in Figures 1 and 2.

Example 1

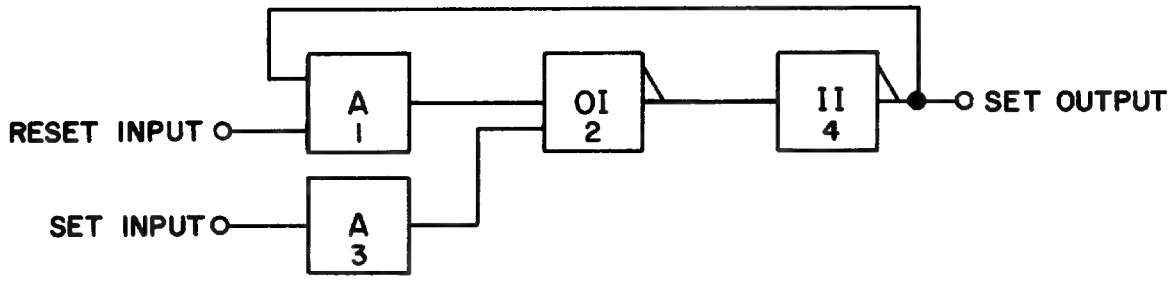
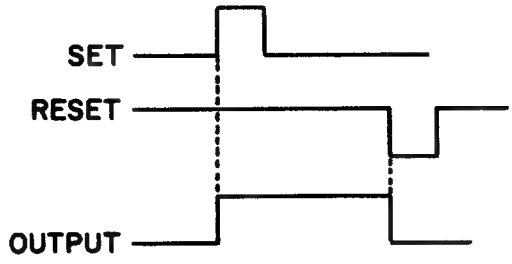


Figure 1. Set-reset latch using an AOI, AOX, Inverter combination.

Note: Logic block 1 and 2 is an AOI
Logic block 3 is an AOX
Logic block 4 is an II

Typical Waveforms



Operation- The set input is normally down and the reset input normally up. Raising the set input to a logical "1" will set the latch output (set output) to a logical "1". This set output is fed back and ANDed with the normally up Reset Input to hold the latch on. The Set Input may now be returned to its normal logical "0" level without disturbing the latch. Dropping the Reset Input to a logical "0" will reset the latch and return the Set Output to a logical "0".

Example 2

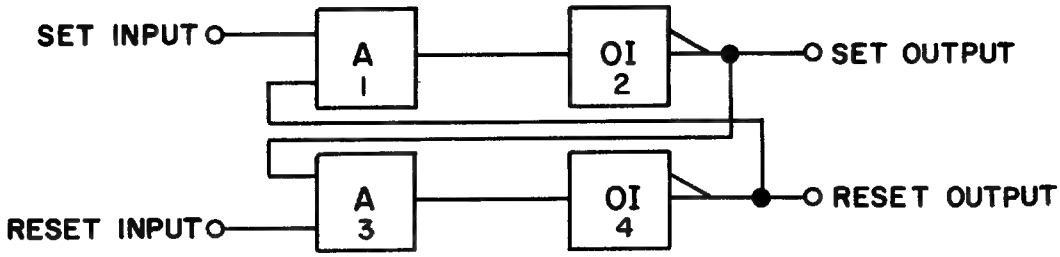
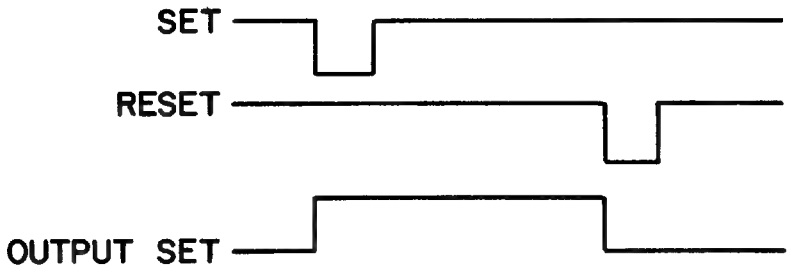


Figure 2. Set Reset Latch using two AOI's

Typical Wave Forms



OPERATION- In this latch both Set and Reset inputs are normally at a logical "1". Dropping the Set Input to a logical "0" will set the latch and bring the Set Output to a logical "1". The latch may be reset by bringing the Reset Input to a logical "0".

Additional Inputs:

Additional Set and Reset inputs may be added to either latch.

In Example 1, Reset Inputs can be added by AND extending block 1, with FDD's, and Set Inputs can be added by additional AOX inputs to block 2.

In Example 2, additional Set and Reset inputs are obtained by AND-extending blocks 1 or 3 with FDD's.

5.4 Exclusive-OR Configurations

A Boolean expression commonly used to describe a two way exclusive-OR (XOR) is written as $A \veebar B$. In the SLT technology there is one module (P/N 841577) in the A family which yields the exclusive-OR function directly. However, when an exclusive-OR function is desired in the remaining families the designer must assemble it by combining elementary building blocks.

1.) Exclusive-OR

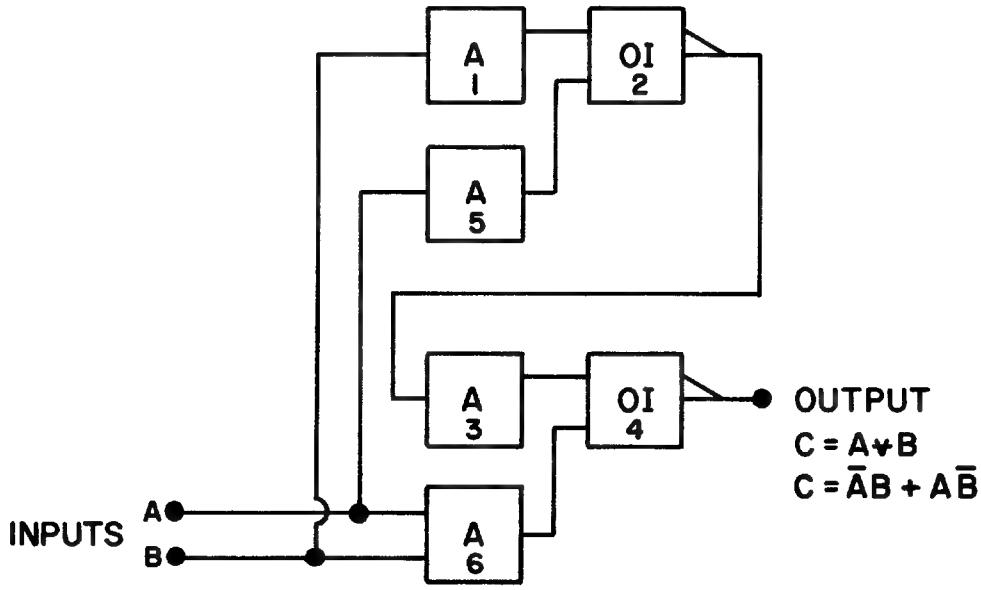
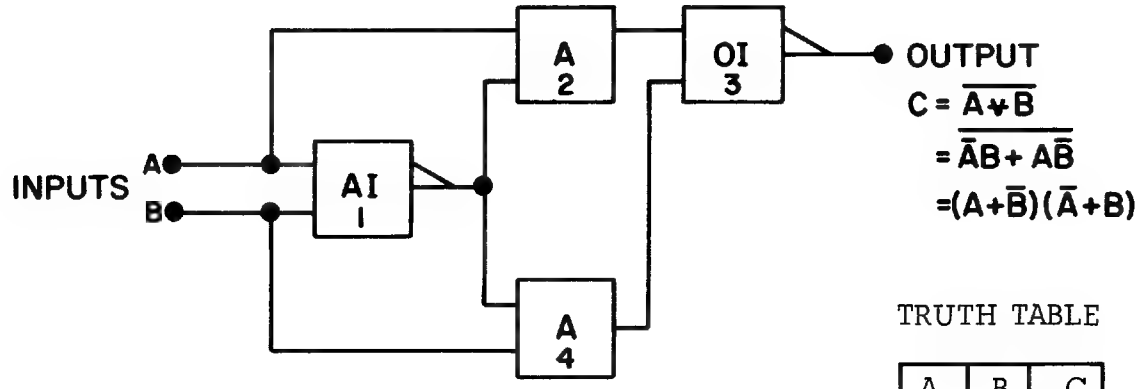


Figure 3. Exclusive-OR Configuration

Note: Logic blocks 1 and 2, 3 and 4, are AOI modules.
Logic blocks 5 and 6 is an AOX module.

Operation
The output of this circuit is "1" when only one of the inputs is up.

2.) Complemented Exclusive-OR



TRUTH TABLE

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

Figure 4. Complemented exclusive-OR configuration.

1 is the most positive up level; 0 is the most negative down level.

Note: Logic block 2 and 3 is an AOI module.
Logic block 1 is an AI.
Logic block 4 is an AOX module.

Operation:
The output of this circuit is one when both inputs are at the same logical level.

Additional complex functions useful in logic design can be designed around the exclusive-OR configuration. A Half Adder as well as Parity Generators, for example, can readily be realized using exclusive-OR circuits.

5.5 Half Adder

A half adder circuit is generally used for adding two binary digits. This circuit has two inputs, the two binary digits to be added, and two outputs, the sum and the carry. One of the several ways this circuit can be implemented, using SLT, is by adding two inverters to the previously discussed exclusive-OR configuration.

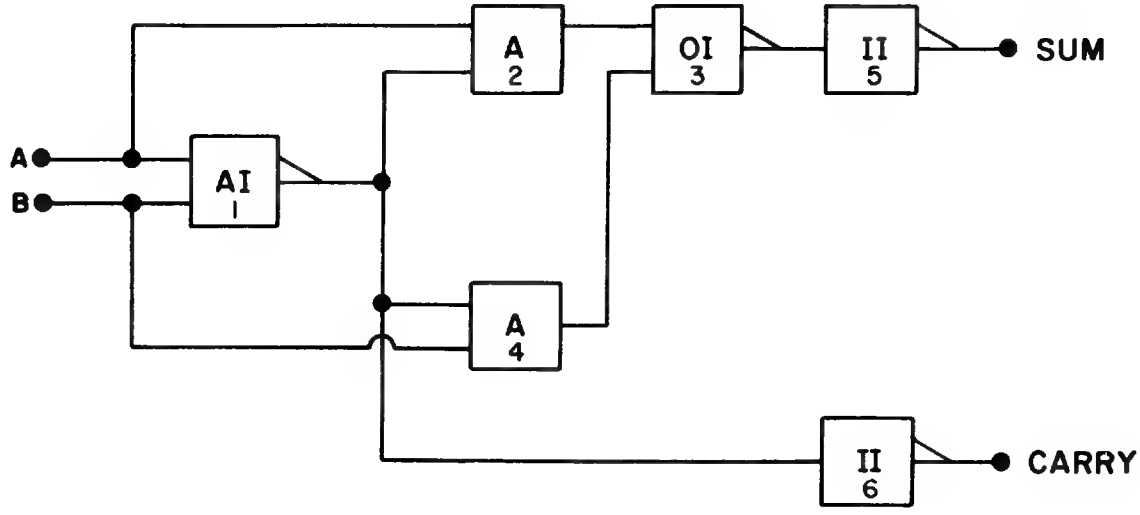


Figure 5. Half Adder

Truth Table

A	B	SUM	CARRY
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

5.6 Parity Generators

Parity generators serve to indicate if an odd or even number of lines are in the same state. This logic function can be realized by connecting a number of exclusive-OR circuits in the pyramid-like arrangement shown in Figure 6.

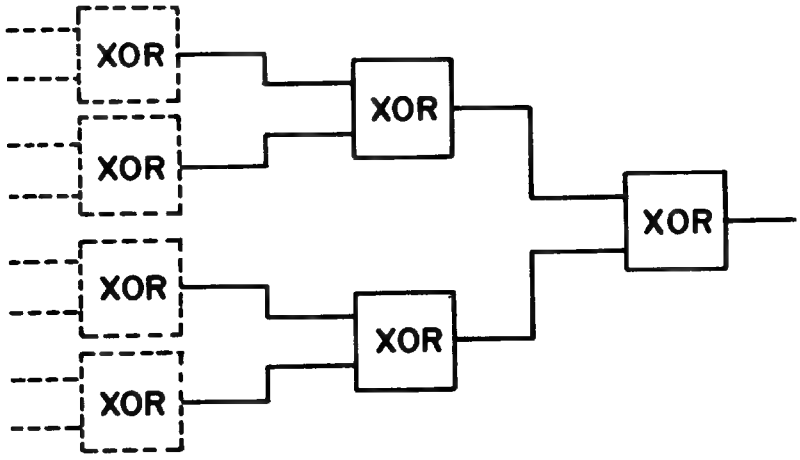


Figure 6. Parity Generator

In the SLT family A, this function can be obtained using the exclusive-OR (module P/N 841577). In the other SLT families the function would be assembled using the basic A-O-I modules in the XOR configuration described earlier.

An example of a four-input even-parity generator, using basic A-O-I- modules, is shown below.

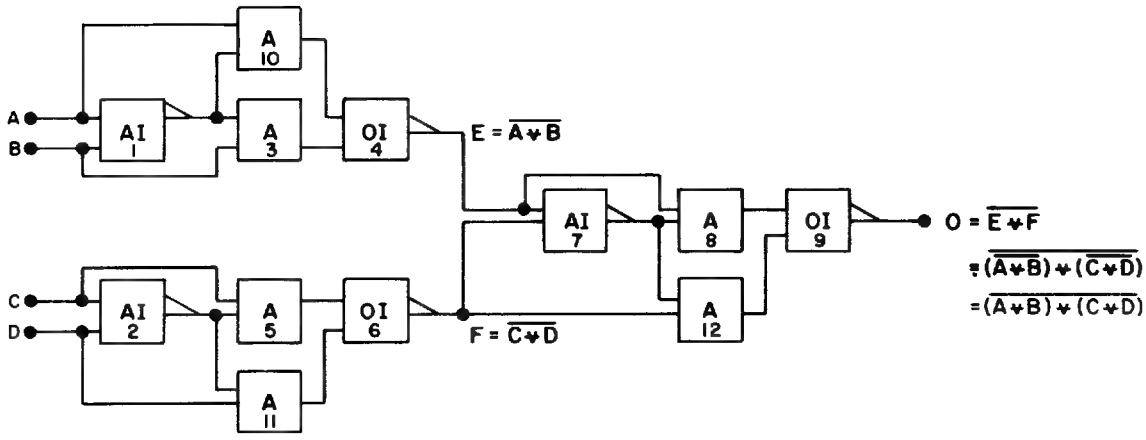


Figure 7. Even Parity Generator

Note: Logic blocks 3 and 4, 5 and 6, 8 and 9, are AOI modules.
Logic blocks 1, 2 and 7 are AI modules.
Logic blocks 10 and 11, and logic block 12 are AOX modules.

Operation: (Even)

The output of this circuit is up when either none, two, or all four of the inputs are up.

Truth Table

A	B	C	D	Output
0	0	0	0	1
1	0	0	0	0
0	1	0	0	0
1	1	0	0	1
0	0	1	0	0
1	0	1	0	1
0	1	1	0	1
1	1	1	0	0
0	0	0	1	0
1	0	0	1	1
0	1	0	1	1
1	1	0	1	0
0	0	1	1	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

5.7 Full Adder

The full adder, like the half adder, is generally used to perform binary addition. The only difference between a half adder and a full adder is that the full adder provides for a carry input whereas the half adder does not.

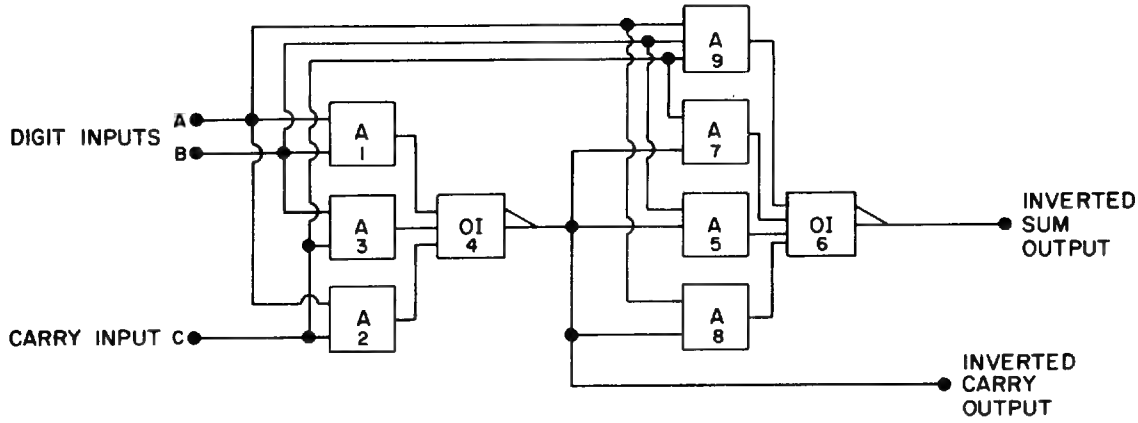


Figure 8. Full Adder

Note: Logic Blocks 3 and 4, 5 and 6, are AOI modules.
Logic Blocks 1 and 2, 7 and 8, and 9 are AOX modules.

Operation: This full adder generates the inverted sum and the inverted carry outputs of the digit inputs. If the inverted inputs and inverted carry input are used, the sum and carry will be outputs.

Truth Table

INPUTS			INVERTED	INVERTED
A	B	C	Sum	Carry
0	0	0	1	1
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
1	0	1	1	0
0	1	1	1	0
0	0	1	0	1
1	1	1	0	0

5.8 Parallel Adder

A number of full adders can be connected together to form a parallel adder as shown in Figure 9.

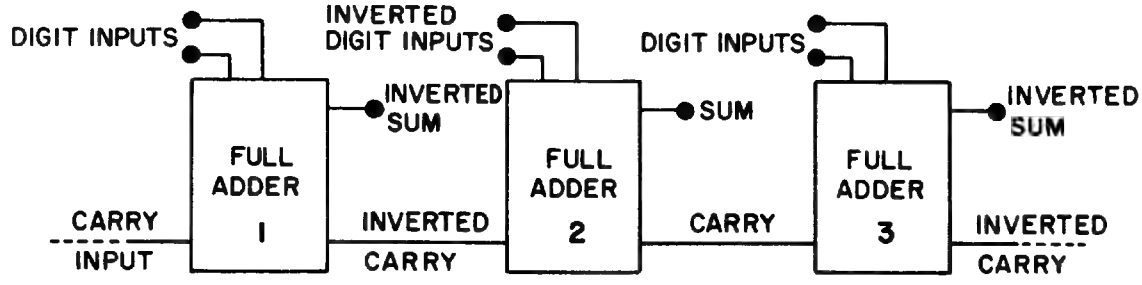


Figure 9: Parallel Adder

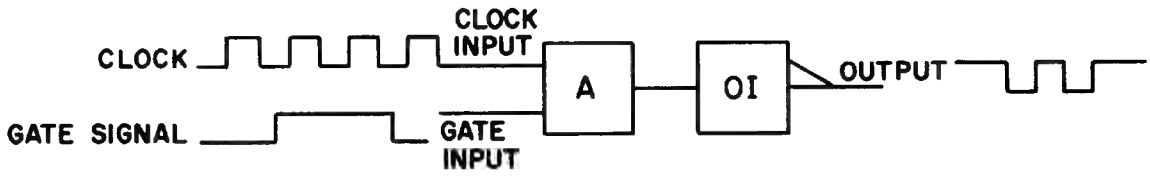
Note: Full adders 1, 2, and 3 are identical. See Figure 8 for circuit diagram.

Operation: This parallel adder provides alternate sum and inverted sum outputs from the inverted digit and digit inputs respectively.

5.9 Gated Clock Signals

In logic design it sometimes is desirable to transmit a series of pulses according to a signal. The easiest way to achieve this operation is to simply use an elementary gate.

In this circuit the gate signal controls the length of time of observable clock output. This design has limited applications because the gate signal may come up in the middle of a positive clock pulse. A way around this is to time the gate signal using other signals available in the system so as to make the gate signal change state only when the clock pulse is down. When the gate signal is random and there are no useful timing signals available in the system, the clock input itself can be used to allow a train of complete clock pulses to be transmitted. This is called random clock gating.



5.10 Random Clock Gating

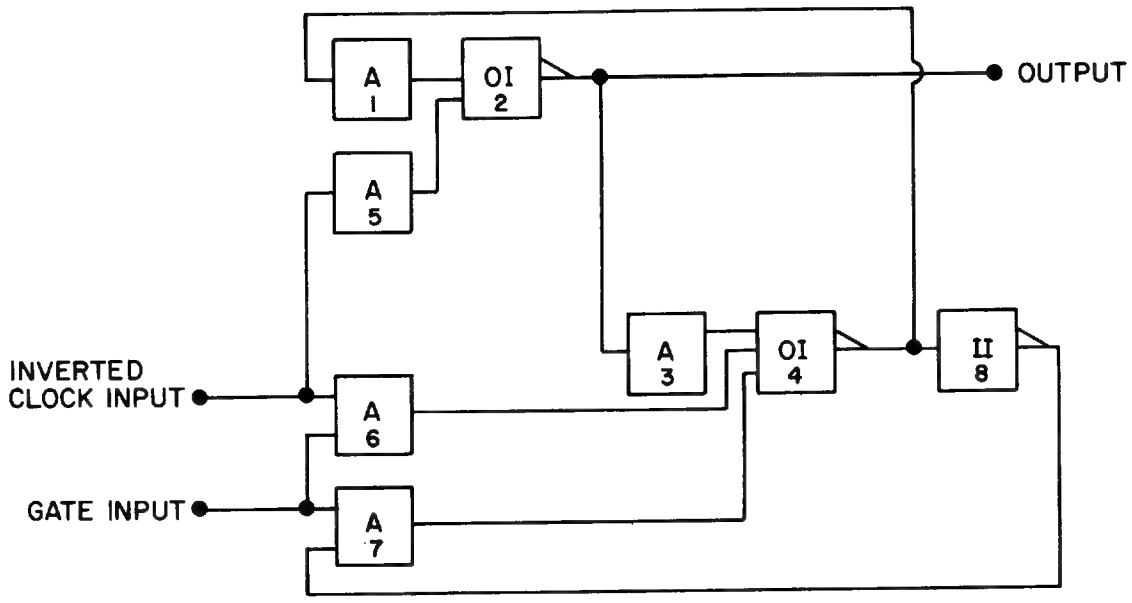


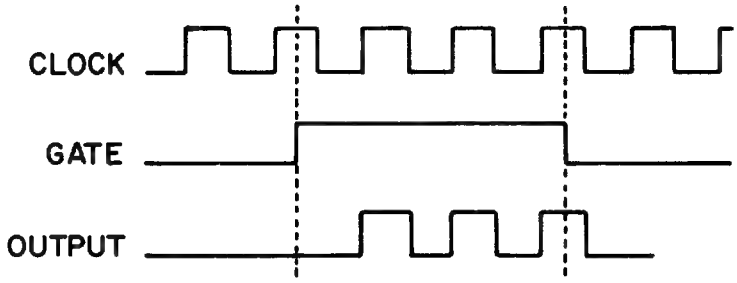
Figure 10: Random Clock Gating

Note: Logic blocks 1 and 2, 3 and 4 are AOI module.
Logic blocks 5, 6 and 7 are AOX modules.
Logic blocks 8 is one-half of an II module.

Operation:

This circuit uses a single inverted clock input. The gate input is normally down and must be raised to gate the clock signal. This circuit will transmit a train of complete clock pulses beginning with the first clock pulse which rises after the gate signal rises, and ends with the last clock pulse which rises before the gate signal falls. The output will fall when the clock signal falls; therefore, the output can only fall at the end of a clock signal. This circuit will gate a clock signal without shortening any of the clock pulses, regardless of the gate signal timing.

Typical Waveforms



5.11 Non-Overlapping Inverters

The circuit shown in Figure 11a generates true and inverted outputs, and its logical "0" levels do not overlap. Neither output can fall until after the other output rises.

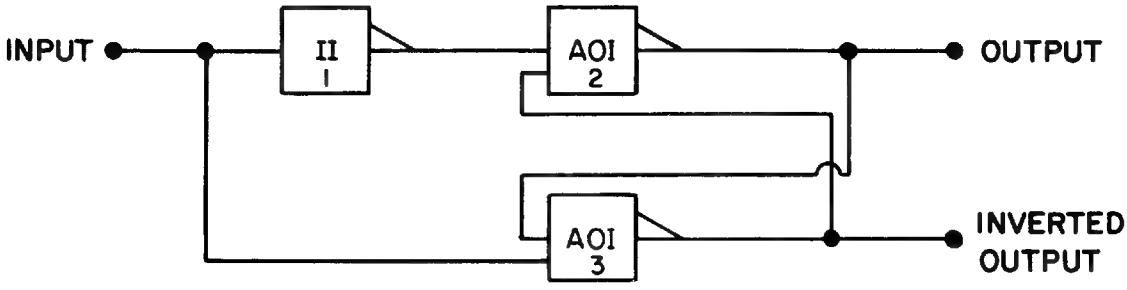


Figure 11a: Non-Overlapping Inverter, Down-Levels

Note: Blocks 2 and 3 are AOI modules.
Block 1 is an II module.

For non-overlapping up-levels the circuit shown in Figure 11b may be used. Neither output can rise until after the other output falls.

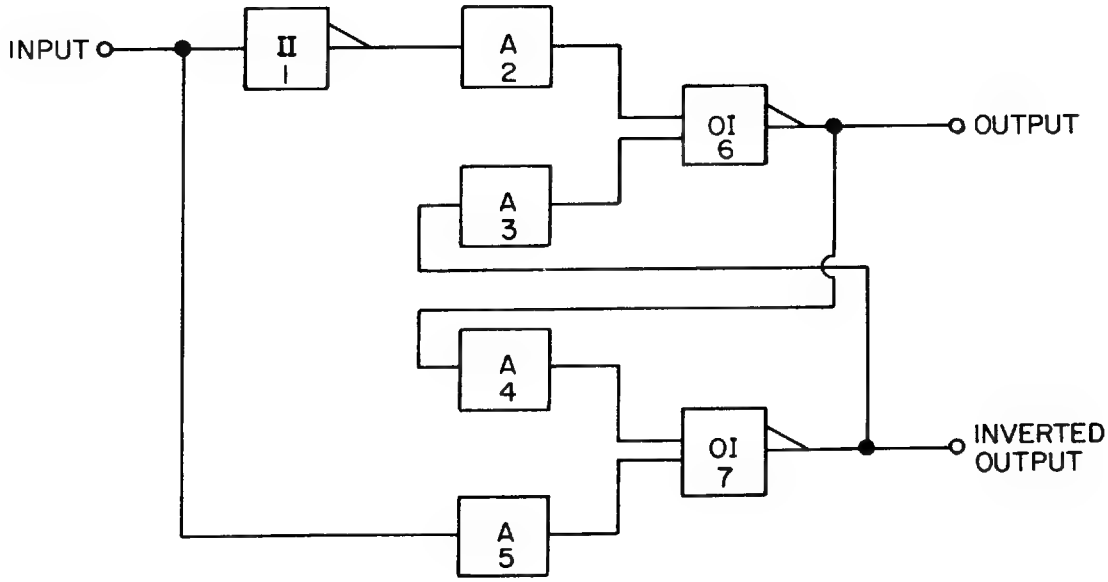


Figure 11b: Non-Overlapping Inverter, Up-Levels

Note: Block 1 is an II module. Blocks 2 and 6, 4 and 7 are AOI modules. Blocks 3 and 5 are AOX modules.

The output signals follow the input in both circuits except for transients during switching.

The usefulness of these circuits stems from the occasional need for non-overlapping true and complemented logic signals in avoiding hazards.

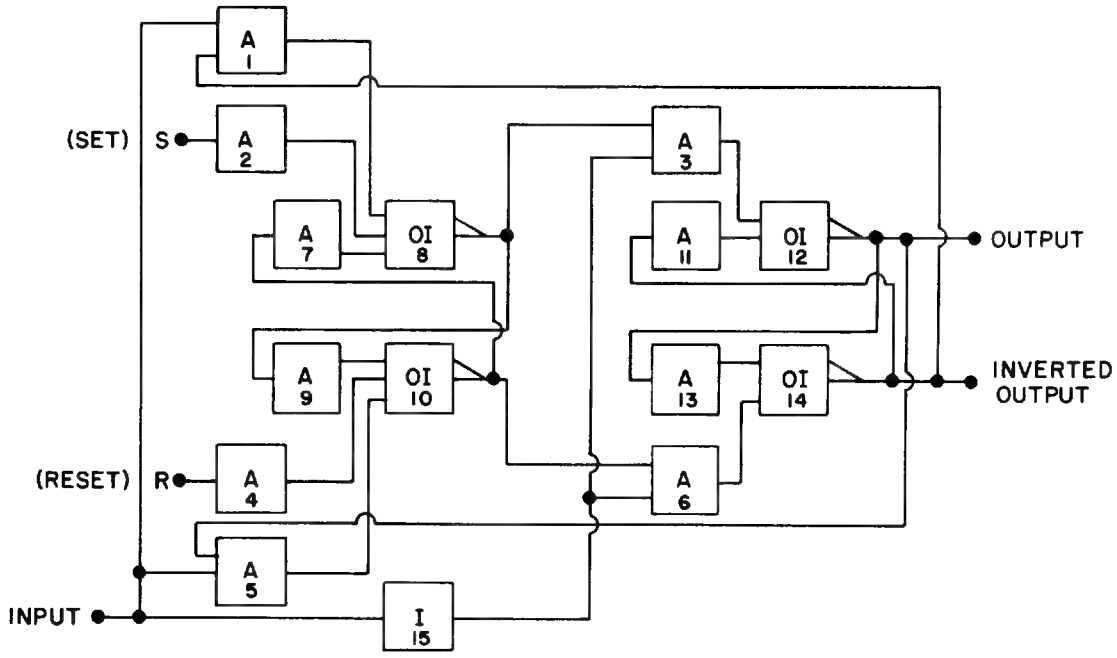


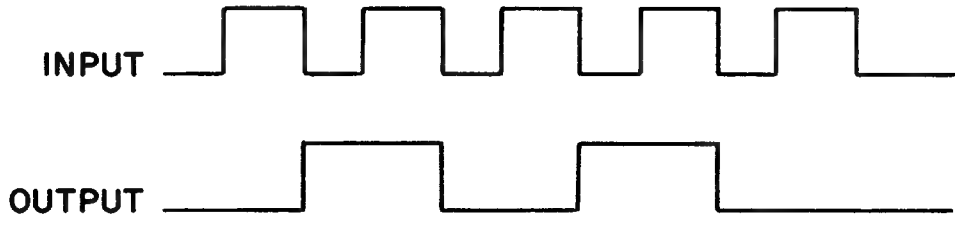
Figure 12a: D. C. Binary Trigger #1

Note: Logic blocks 1 and 2, 4 and 5, 3 and 6 are AOX modules.
Logic blocks 7 and 8, 9 and 10, 11 and 12, 13 and 14 are AOI modules.
Logic block 15 is an II module.

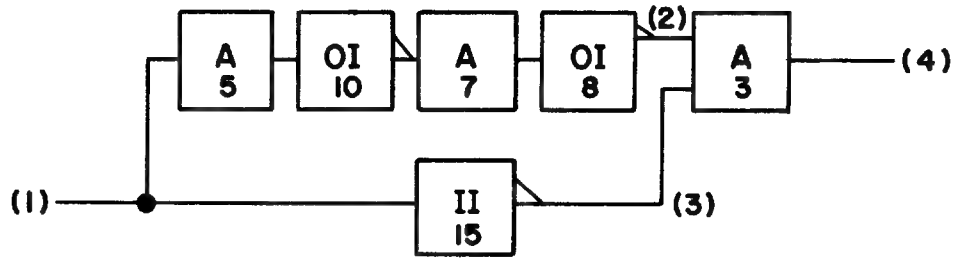
Operation:

The set and reset inputs, which are normally down, can be used to set or reset the first latch into the desired state by bringing up the corresponding input momentarily.

Every time the input goes down the information stored in the first latch is shifted into the second latch in an inverted form. Every time the input goes up the information stored in the second latch is shifted into the first latch. The output can only change state during the downward transition of the input signal. The waveforms shown summarize typical trigger operation.



Using the inverter as shown, the circuit contains the following hazard:



When (1) rises, (2) may rise before (3) falls, causing an unwanted positive pulse at (4). If an inverted input is used instead of an inverter, the hazard will depend upon the overlap of the two signals. This hazard can be removed from this trigger through the use of the nonoverlapping inverter circuit (circuit 11b) by using the true and complemented outputs as the driving signals and removing inverter block 15.

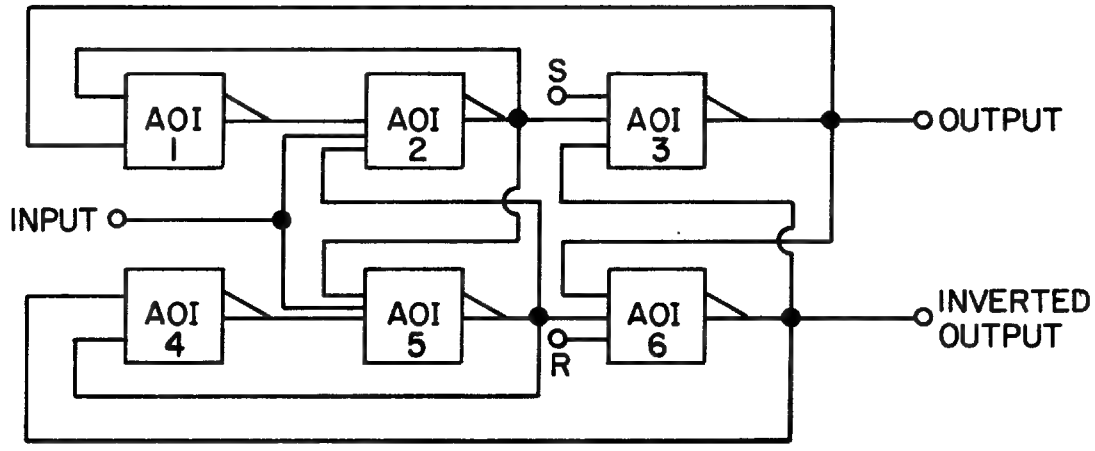


Figure 12b: D. C. Binary Trigger #2

Note: Logic blocks 1, 2, 3, 4, 5, and 6 are AI modules.

Operation: This is a very reliable binary trigger. Its operation is relatively independent of the delay through any of its blocks.

The S and R inputs are normally up. The trigger may be set or reset by bringing down S or R, respectively, when the input is down.

The output changes state on each rise of the input signal.

5.13 Storage Registers

Storage registers are generally used as a short time memory. Information is entered into a storage register and is held there while it is being operated upon.

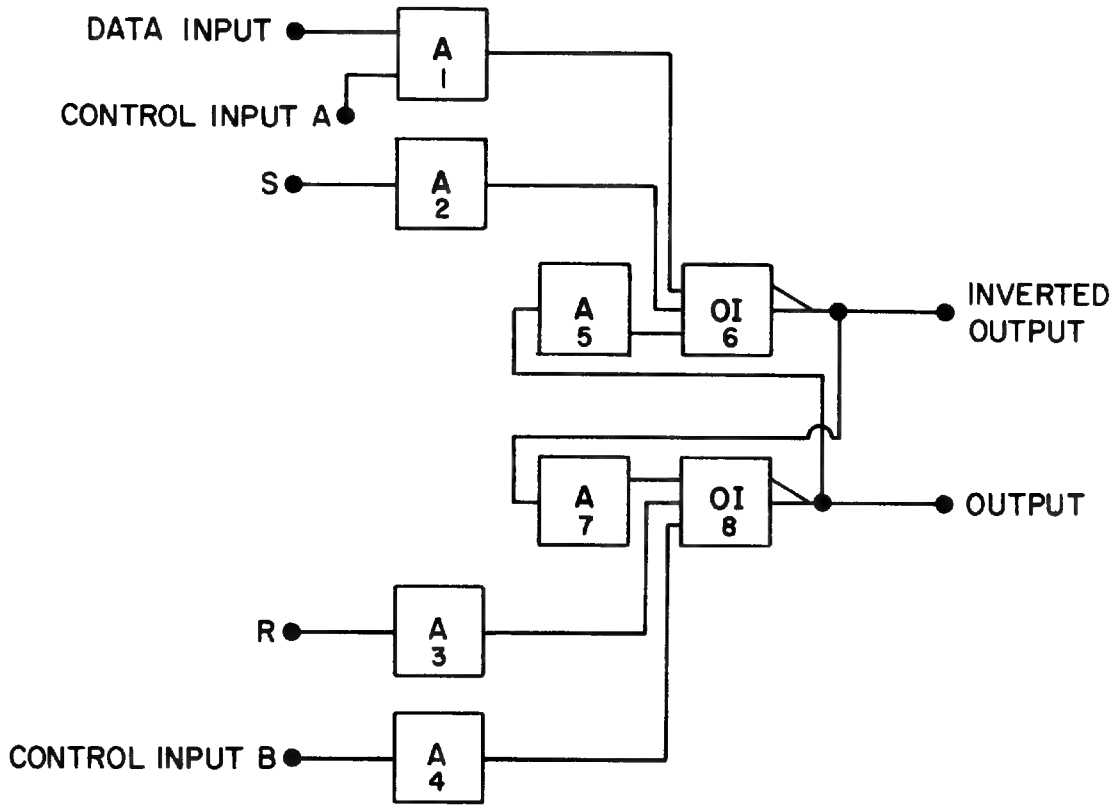


Figure 13a: Storage Register #1

Note: Logic blocks 1 and 2, 3 and 4 are AOX modules. Logic blocks, 5 and 6, 7 and 8 are AOI modules.

Operation:
This register requires two control inputs and one data input.

Control Inputs: Control inputs A and B are normally down. When entering data, B is raised to reset the registers, then A is raised. Control input B must then be lowered before A is lowered. Control signal A may be obtained from control signal B by the use of a delay.

Data Input: The value of the data input does not affect the register while control input A is down. When A is up the value of the data is entered into the register. The data signal should not change while control input A is up and B is down. If the value of the data to be entered into the register is available in inverted form only, then the inverted output would be used rather than the true output.

Set and Reset Inputs: The Set and Reset inputs are normally down. Any register position may be set or reset by raising S or R, respectively while A and B are down.

Additional Inputs: Additional data lines may be gated into the register by using a separate pair of AND gates for each data input. The additional data lines can be obtained by OR extending logic blocks 2 & 4 with an AOX module. Only one data line may be activated at any time. Additional control signals are required to select the proper gates.

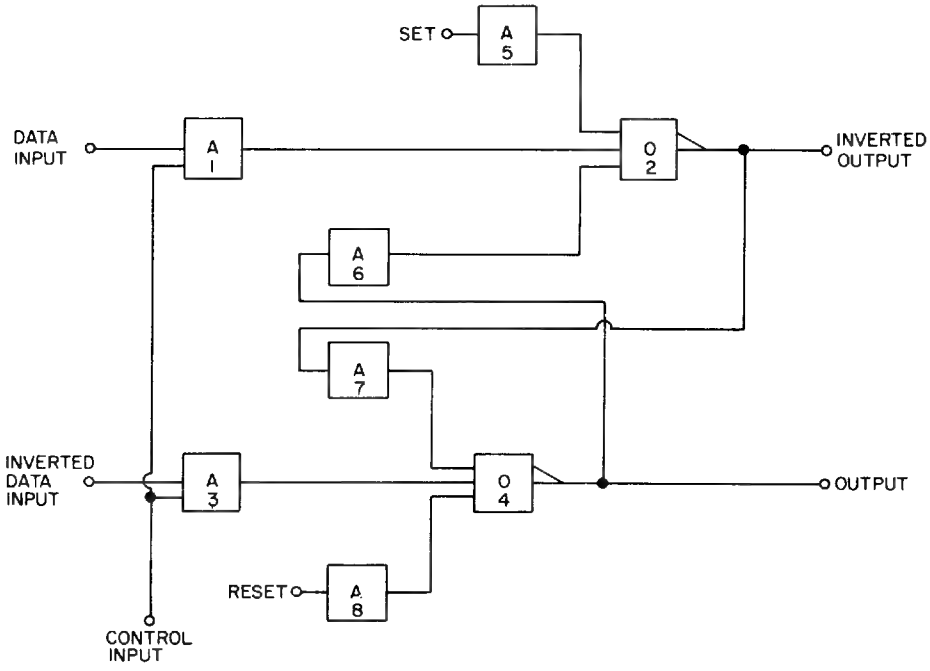


Figure 13b: Storage Register #2

Note: Logic blocks 1 and 2, 3 and 4 are AOI modules.
Logic blocks 5, 6, 7, and 8 are AOX modules.

This register uses a single control input but requires both true and complemented data inputs. The control input is normally down but is raised when entering new data into the register.

The value of the data input signals does not affect the register when the control input is down. The data may be changed while the control input is up but must reach its final value before the control input is lowered.

5.14 Shift Register

A shift register consists of a number of storage units interconnected in such a way that the information stored in one unit can be transferred to the following stage through the use of a control signal. A two stage shift register using the storage register of Figure 13b is shown below.

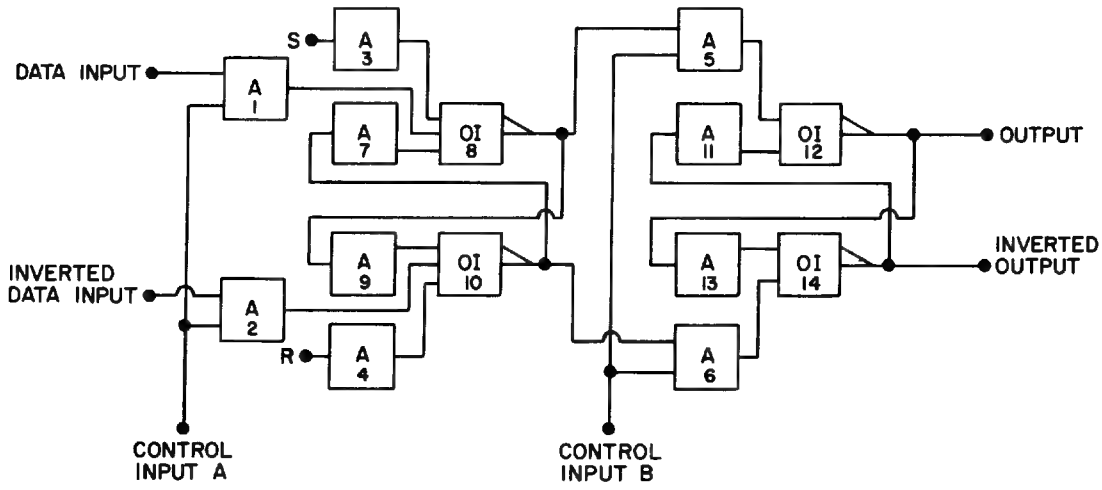


Figure 14: Shift Register (Two Stages)

Note: Logic blocks 1 and 2, 3 and 4, 5 and 6 are AOX modules. Logic blocks 7 and 8, 9 and 10, 11 and 12, 13 and 14 are AOI modules.

Operation:

Set and Reset Inputs: The S and R inputs are normally down. Any register position may be set or reset by raising S or R, respectively, while control input A is down and control input B is up.

Circuit Requirements: This shift register requires two control inputs, and both true and inverted data inputs.

Control Inputs: Control inputs A and B are normally down. To begin a shift, control input A is raised to enter data into the first latch. When the first latch is set, A is brought back down and B is raised to enter the data into the second latch. Bringing down B completes the shift.

Control input B can be obtained by inverting control input A, or vice versa, but this can result in a hazard since both control inputs would transiently be up at the same time. If the nonoverlapping inverter (Figure 11b) is used to feed control input A and B, the hazard is removed.

Data Input: The value of the data input is entered into the register when A is up. The data may be changed while A is up, but it must reach its final value before A is lowered. The inverted data input must have the opposite value at this time.

Output: During shift operation, the output changes to its new value when B is raised.

Additional Inputs: Each additional pair of data inputs requires an additional pair of AND gates, obtained by OR extending logic blocks 8 and 10 with an AOX module. True and inverted data inputs must be connected to these AND gates and additional control signals are necessary to select the desired input. Only one pair of gates may be activated at any time.

5.15 Ring Circuit

A ring circuit consists of a sequence of interconnected storage units arranged such that only one output is up at a time. The control signals from one or sometimes two control inputs, cause the "1" state to propagate down the sequence.

Ring circuits are commonly used to distribute timing signals to control sequentially other logic circuits. The may also be used as counters since the position of the last raised output is an indication of the number of control sequence operations received by the circuit.

Rings may be open or closed. In an open ring, the output sequence begins at the first stage and ends at the last stage and does not begin again until the ring is reset. In a closed ring the last stage is connected back to the first stage, and the output sequence can cycle around the ring continuously.

To initialize a ring, all stages but one should be reset by means of the R input, and one stage should be set by means of the S input.

Ring Circuit (Con't.)

Any shift register can, in general, be used as a ring if a single "1" bit is entered into it. The ring circuit shown below cannot, however, be used as a shift register.

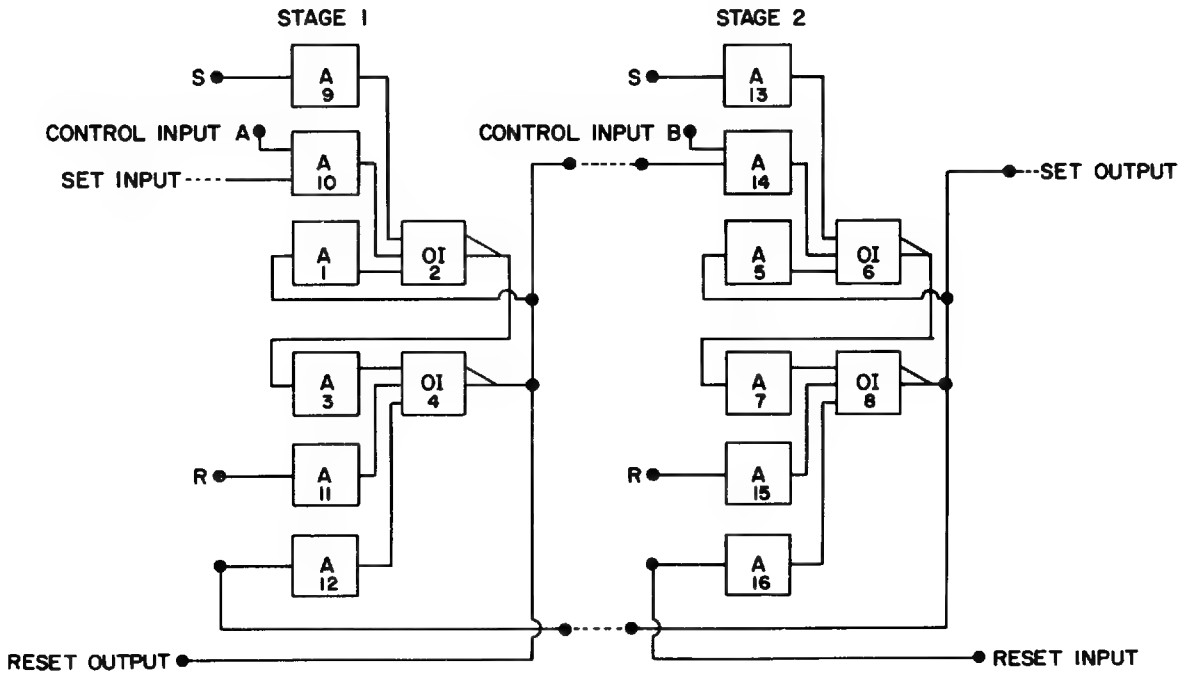


Figure 15: Ring Circuit (Two Stages)

Note: Logic blocks 1 and 2, 3 and 4, 5 and 6, 7 and 8 are AOI modules. Logic blocks 9 and 10, 11 and 12, 13 and 14, 15 and 16 are AOX modules.

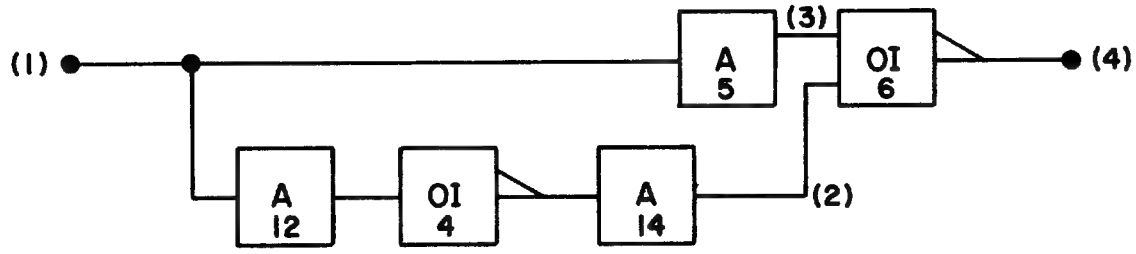
Operation:
This circuit requires a single set line and a single reset line between stages. It uses two control inputs which are connected to alternate stages.

Control Inputs: Control inputs A and B are normally down. When operating the ring, these signals are alternately raised, i.e., A is raised and lowered, then B is raised and lowered, then A is raised and lowered, etc. Each time A or B is raised, a new output comes up. It is possible to obtain signal B by inverting signal A, and if a nonoverlapping inverter is used, the hazard of signal overlap is avoided. When both signals are up at the same time, the signal overlap may cause the ring to operate improperly.

Outputs: The output of the lower AOI blocks serves as the output of each stage. The line will come up when the stage is set, and fall when the following stage is set. The output of the upper AOI serves as the inverted output of each stage.

Set and Reset Inputs: The S and R inputs are normally down. A stage may be set or reset by raising S or R respectively.

Hazard: The circuit contains a hazard which is shown in the partial circuit diagram below:



Assume that (1), (3), and (4) are down, and that (2) is up. (1) rises causing (3) to rise and (2) to fall. If (2) falls before (3) rises, an unwanted positive pulse appears at (4).

5.16 Serial Binary Counter

Figure 12a, the D. C. Binary Trigger circuit of Section 5.12 may be used to construct a Serial Binary Counter. Each stage of the Serial Binary Counter is one complete D. C. Binary Trigger. The stages are connected in series with the Output of one stage driving the Input of the next as shown in Figure 16.

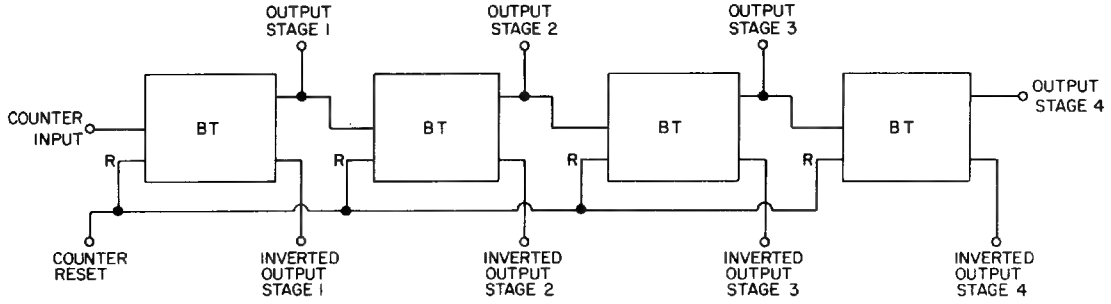


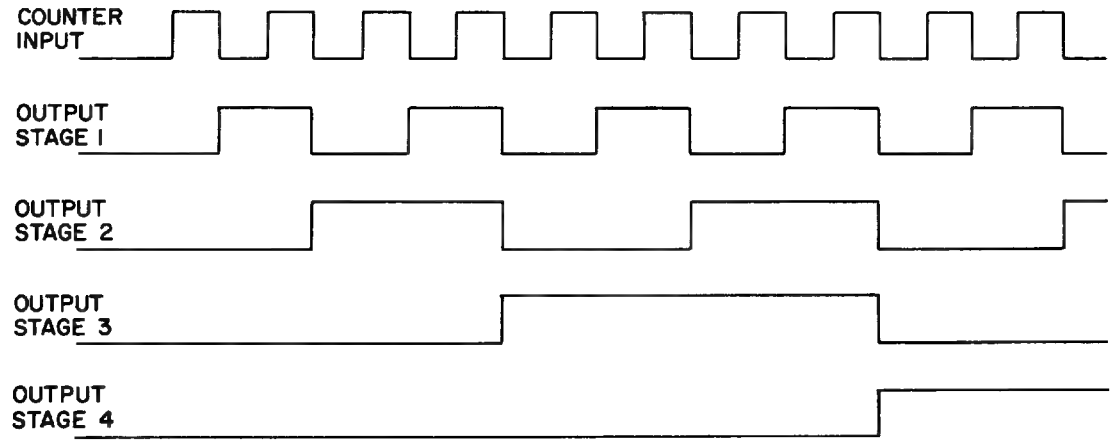
Figure 16a: Serial Binary Counter (4 Stages)

Operation: when counter is built using the circuit of Figure 12a:

The Counter Input is normally down, and each rise and fall of the Input will increase the count by one. The Counter Input drives the first stage only.

The Counter may be reset by bringing down the Counter Input and bringing up the Reset Input to each stage. This may result in a ripple reset. The Counter cannot be set to an arbitrary value and, therefore, no Set input is shown.

The Waveforms in Figure 16a are:



Serial Binary Counter (con't.)

For simplicity the Inverter of Figure 12a may be removed. In this case, blocks 3 and 6 of Figure 12a must be driven from the Inverted Output of the previous stage, or from the complemented Counter Input in the case of the first counter stage. The hazard described in Section 5.12 still exists and should be considered when selecting a Counter circuit.

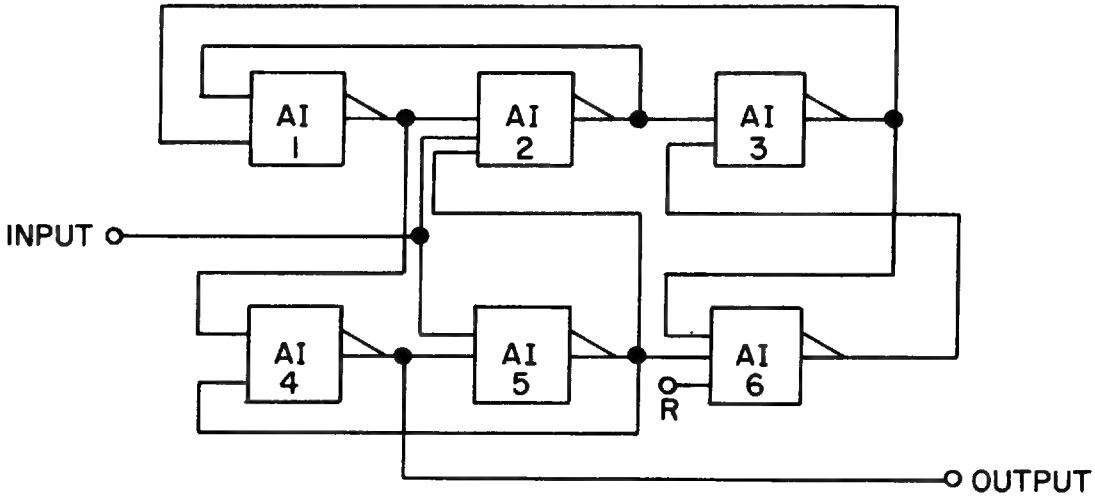


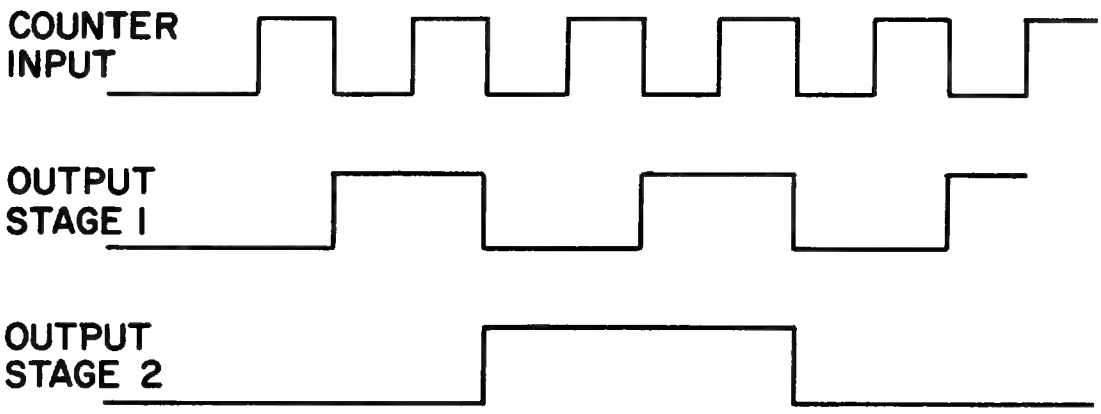
Figure 16b: Serial Binary Counter (1 stage)

Note: All logic blocks are AI modules.

Figure 16b is a high reliability serial binary counter stage. The Counter Input drives the first stage only. Succeeding stages are connected in series, with the output of one stage driving the input of the next.

This counter can be reset by bringing down the Counter Input and bringing down the Reset input to each stage. This may result in a ripple-type reset. Since the counter cannot be set to an arbitary value, there is no Set Input shown.

The Counter Input is normally down. Each rise and fall of the Counter Input will increase the count by one. Typical waveforms for a two stage counter are.



5.17 Bi-Directional Counter

The circuit shown in Figure 17 will convert a series of pulses into binary form, counting up or counting down as directed by the control signal.

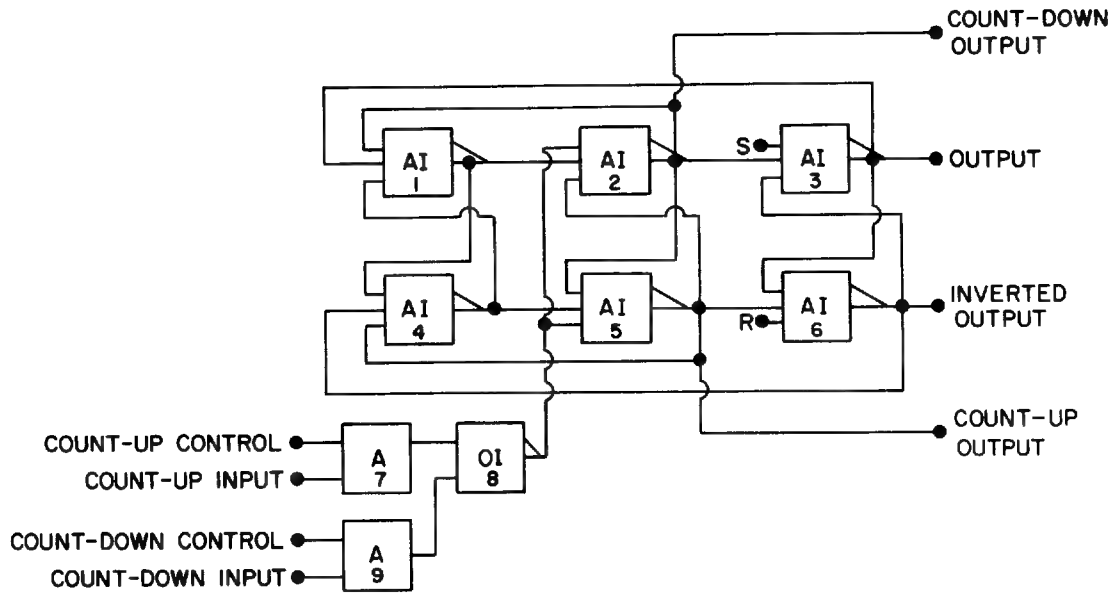


Figure 17: Bi-Directional Counter (one stage)

Note: Logic block 1, 2, 3, 4, 5, and 6 are AI modules.
Logic blocks 7 and 8 are an AOI module.
Logic block 9 is an AOX module.

Operation:

This binary serial counter can count up or down, and its direction may be changed without disturbing the count.

Counter Input- The first stage of the counter does not require the AOI control block. The input is connected directly to the two AI blocks in the middle of the binary trigger circuit. The input signals are normally down. Each rise and fall of the input signal will change the count by 1, the direction of the change being determined by the direction control input.

Direction Control Inputs- The count-up and count-down control lines must be connected to every stage except the first. To count up, the count-up control line must be up, and the count-down control line must be down. To count down, these signals are reversed. The only time these signals have to be changed is when the direction of the count is to be changed. The direction control signals should only be changed when the counter input signal is down.

Interstage Connections- The count-up and count-down outputs of one stage are connected to the count-up and count-down inputs, respectively, of the following stage.

Counter Output- The output line of each stage indicates the value of that stage at all times.

Set and Reset Inputs- The S and R inputs are normally up. To set or reset any stage, lower the S or R inputs, respectively, while the counter input is down.

5.18 Binary Coded Decimal Counter

The binary coded decimal counter will count from 0 to 9 in BCD form and reset to 0 on the tenth pulse supplying a carry pulse to the next BCD counter through the output network.

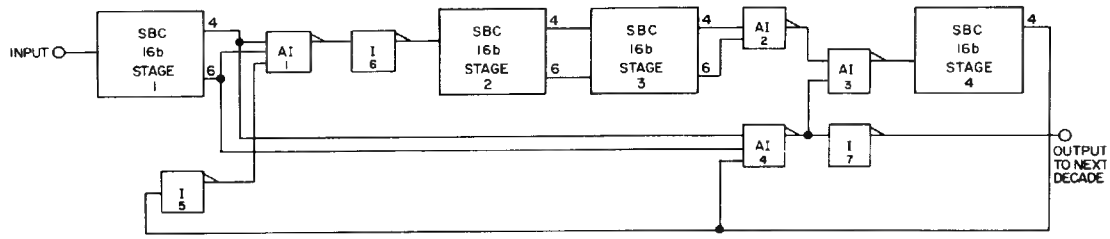


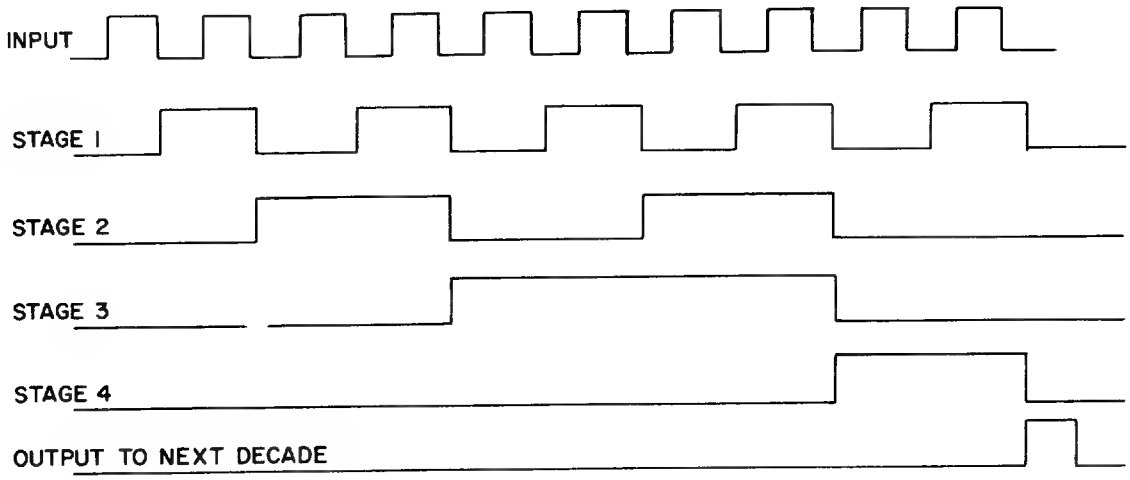
Figure 18: Binary Coded Decimal Counter (one decade)

Logic blocks 1, 2, 3, and 4 are AI modules.
Logic blocks 5, 6, and 7 are II modules.
The 4 logic blocks marked SBC 16b are each identical to the circuit shown in section 5.16, Figure 16b.

This Binary Coded Decimal Counter uses the Serial Binary Counter Stage circuit of Figure 16b as its basic element. Note, in three of the four stages of Figure 18, that two outputs are needed. The numbers 4 and 6 refer to the outputs of logic blocks 4 and 6 in Figure 16b. The second input required by Stage 3 is obtained by extending logic blocks 2 and 5 of Figure 16b with FDD.

Operations:

The Counter Input is normally down. Each rise and fall of the Input increases the count by one. The count in each decade is indicated on four lines, one from each of the 4 binary stages. Typical waveforms when observing the outputs of logic block 3 are:



The inverse of these waveforms is available at block 6. The count is also available at block 4 on the fall of the input signal.

6.0 SLT CIRCUITS ("C" FAMILY - 700 NANOSECONDS)

6.1 A. C. Trigger (P/N 841536)

When working in SLT-700 family, the designer may use the trigger module P/N 841536 to obtain trigger operation or for building latches, registers, binary triggers, ring circuits, shift registers and counters. This trigger is referred to as an AC trigger. In order to use this module, external resistors and capacitors must be used. For a description of the components required, refer to the specifications for P/N 841536.

For all applications, Pins 9 and 16 are connected together, and load resistors R_5, R_6, R_7, and R_8 are externally connected between +12V and the collectors of T_1, T_2, T_3, and T_4 as shown on the specifications.

6.1.1 D. C. Set-Reset Latch

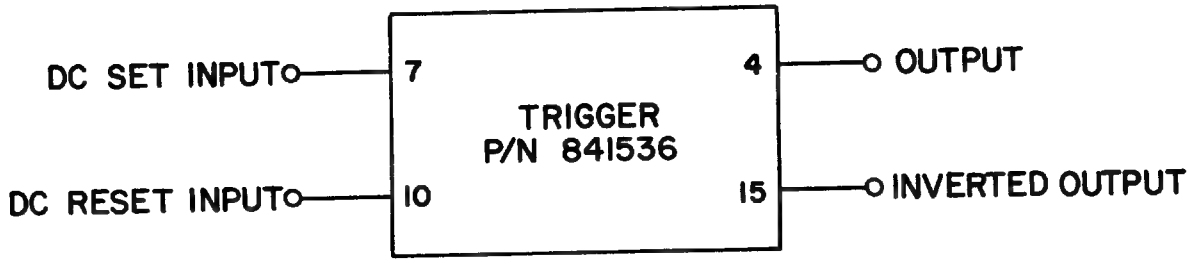


Figure 1: Trigger module used as D. C. Set-Reset Latch.

Operation:

Both the set and reset inputs are normally up. Bringing down the set or reset input will set or reset the latch, respectively. The set output is up when the latch is set and down when the latch is reset. Additional inputs may be added by AND extending pin 12 or pins 9 and 16 with a FDD module.

6.1.2 Storage Register

With the addition of external R. C. networks the trigger module (P/N 841536) can be used as a storage register.

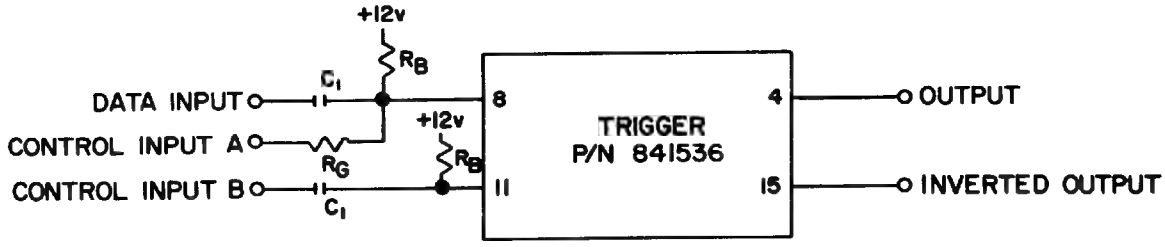


Figure 2: Trigger module connected as a storage register.

See specification P/N 841536 for values of R_B, R_G, AND C_1.

Operation:

Control inputs A and B are normally up. When entering data, control input B is lowered to reset the register. Control input A is lowered to permit the data to affect the register. The data input can only affect the register when A is down. The state of the register only changes during the downward transition of either the data line or control input B. Additional data inputs may be added by the addition of R. C. network to pin 7. Only one R. C. network may be active at a time.

6.1.3 Binary A. C. Trigger

To obtain the binary trigger function the designer must add external R. C. networks to the module.

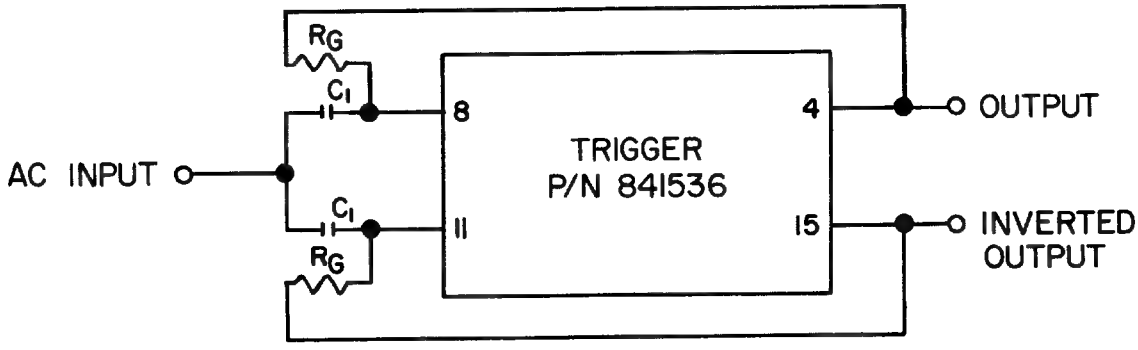
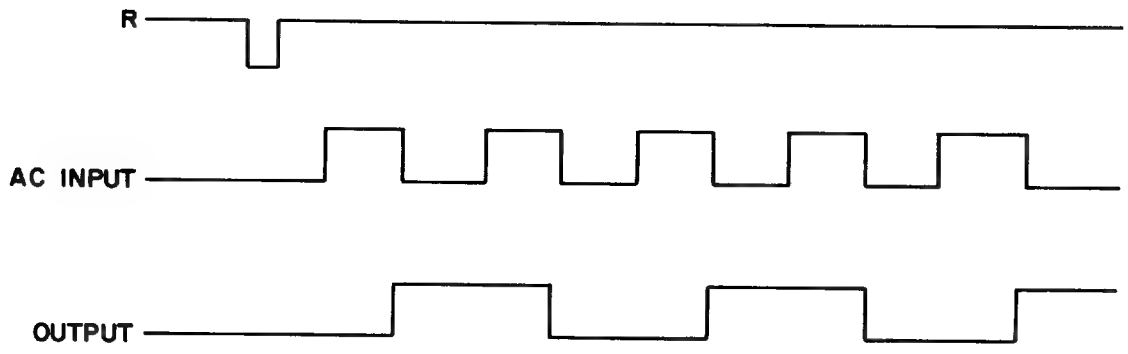


Figure 3: Binary A. C. Trigger
See specification P/N 841536 for values of RG and C1

Operation:

The set (pin 7) and reset (pin 10) inputs are normally up. The register can either be set or reset by lowering S or R, respectively.



6.1.4 Binary Coded Decimal Counter

The connecting of the module as a BCD counter is similiar to that of the asynchronous counter of Figure 5 with the addition of an AI to reset the circuits to 0 on the tenth count.

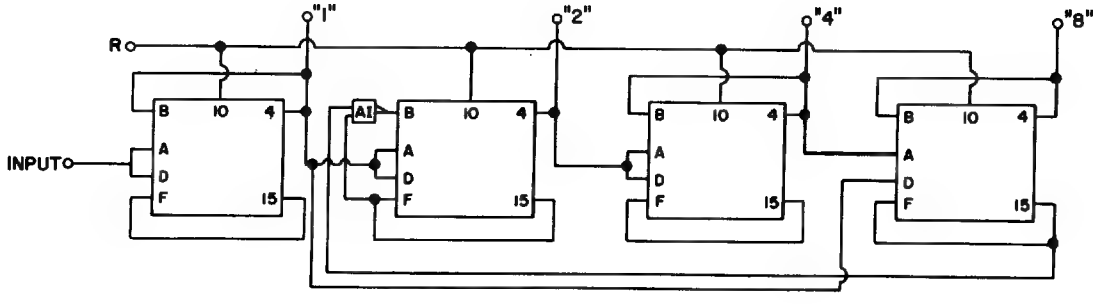


Figure 4: Module P/N 841536 connected as a BCD counter.

6.1.5 Asynchronous Binary Counter

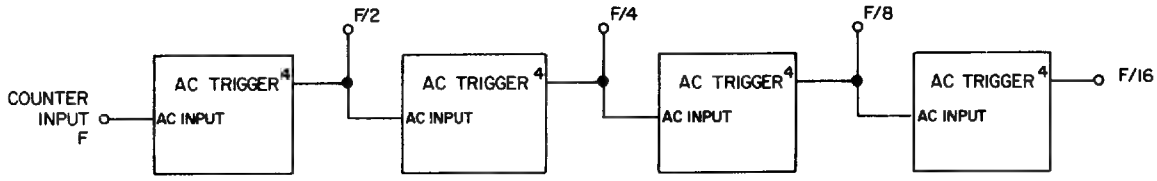


Figure 5: Binary A. C. Trigger connected as a binary counter. See Figure 3 for circuit of Binary A. C. Trigger.

6.1.6 Shift Register

A shift register is a series of storage elements in which bits may be shifted from one element to the next by means of shift pulses. After an input is placed into the register, a shift pulse applied to the shift bus will cause the bit to "shift" to the right.

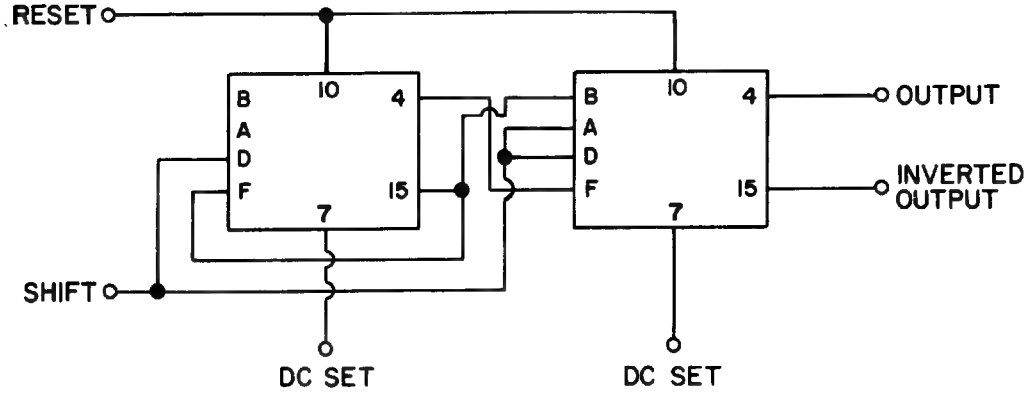


Figure 6: Trigger Module connected as a two-stage shift register

Operation:

The reset bus resets the stages in the shift register. Data is entered into the register by means of the DC Set lines. A shift pulse will then cause the information stored in the register to be shifted to the right.

6.2 Dual AND/OR/Inverter

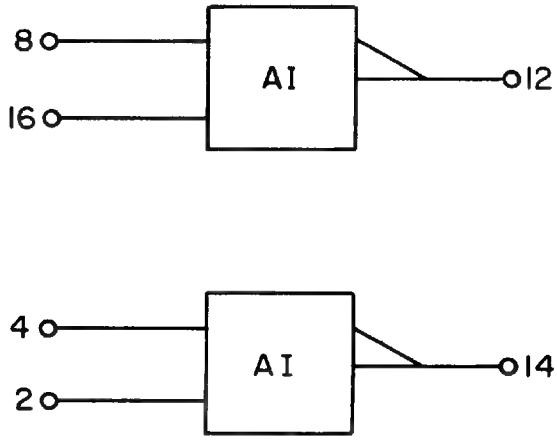


Figure 7: Module P/N 841545 used as two dual input AI's.

This module contains two AOI's which can be used as two-two input AI's by using pins 8 and 16 and pins 4 and 2 as the inputs. When either AOI is OR extended, input pin 16 (or 2) act as though it were an input connected to all the AND gates.

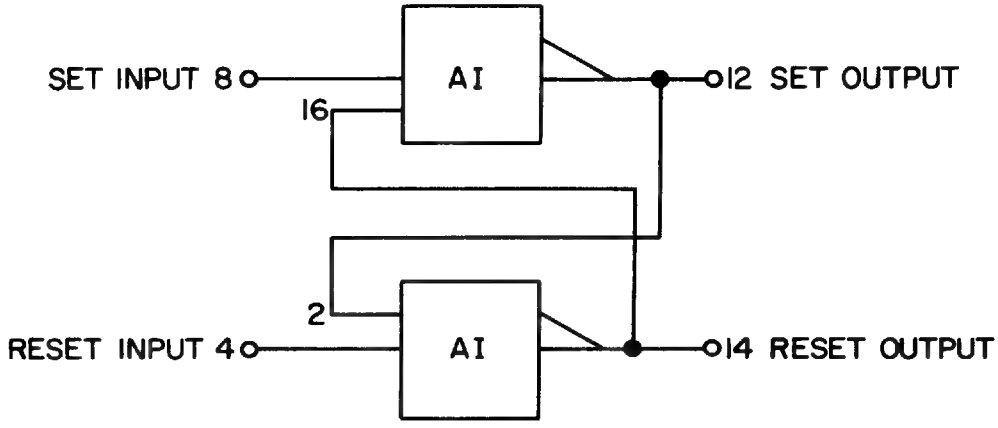


Figure 8: Module P/N 841545 connected as a Set-Reset latch. Operation is the same as the Set-Reset latch of Figure 2 (page E-6)

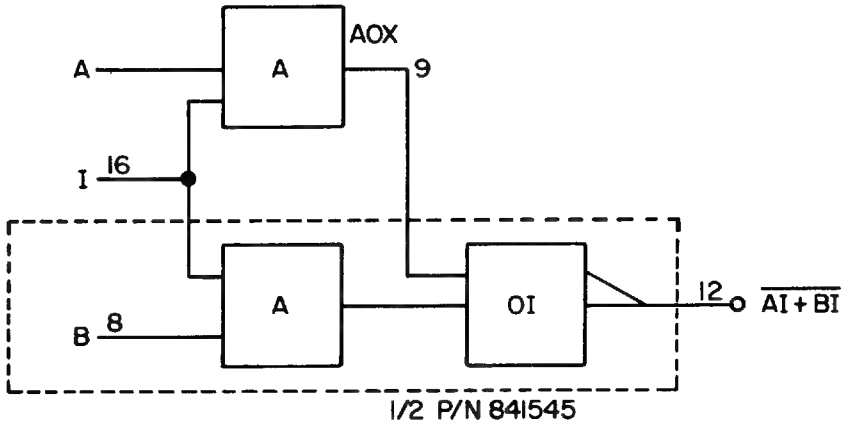


Figure 9: Half of Module P/N 841545 connected as an AOI with an AOX. This is a logical representation of the function. Input I is not physically connected to an input of the AOX.

6.3 Signal Hold Circuit

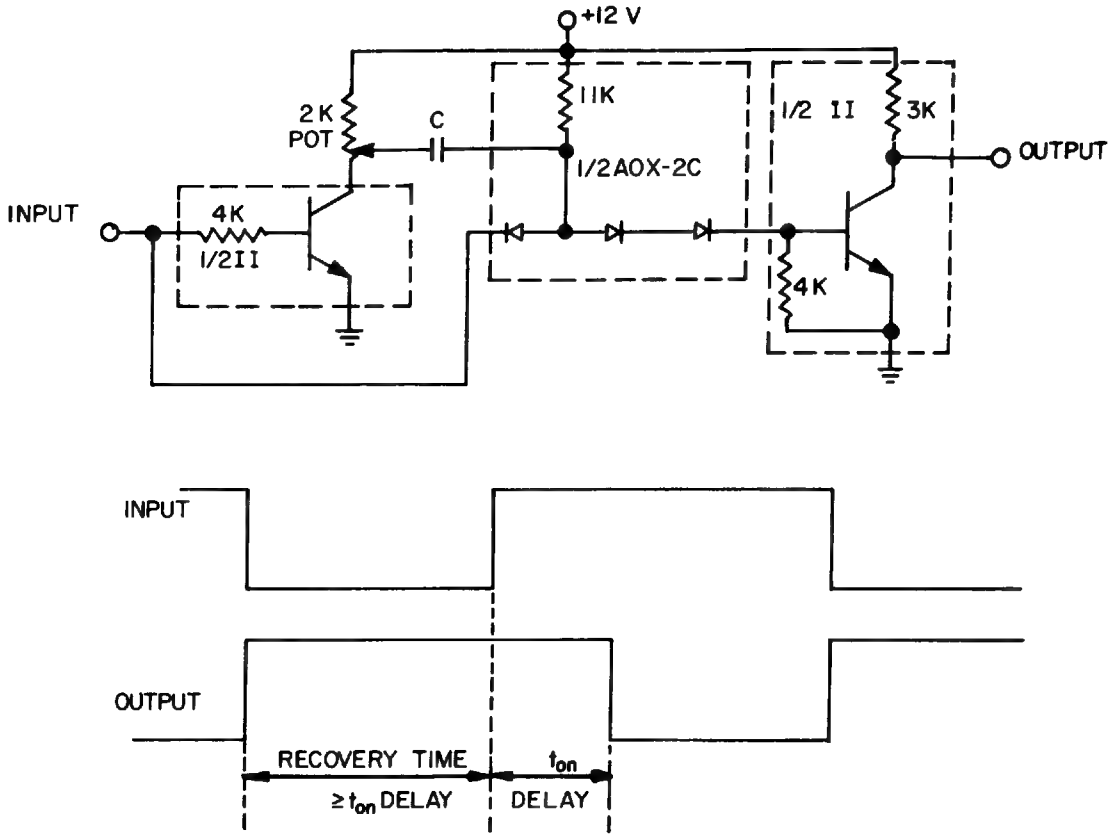


Figure 10

The output signal is inverted and delayed by the T_{on} delay of the circuit. The T_{on} delay is a function of the 2K potentiometer and capacitor C;

Capacitor (μf)	t_{on} delay	
	Minimum	Maximum
0.00068	1.7μs	5.5μs
0.0018	4.5μs	14.6μs
0.0047	12μs	38μs
0.012	30μs	97μs
0.033	83μs	260μs
0.082	205μs	660μs
0.22	550μs	1780μs
0.56	1.4ms	4.5ms
1.5	3.7ms	12ms
3.9	9.7ms	31ms
10	25ms	81ms
27	67ms	220ms

6.4 Single Shot (Variable)

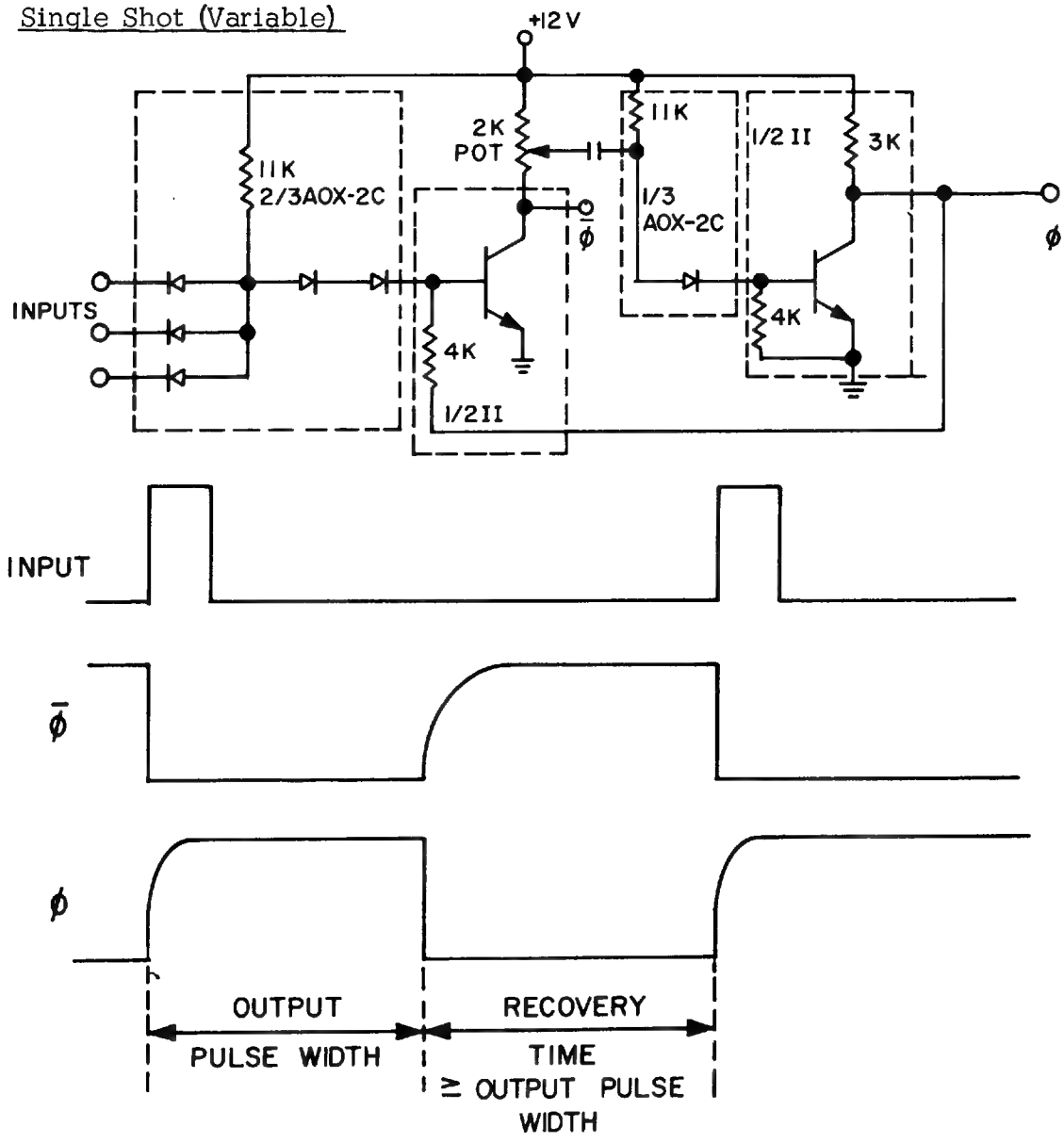


Figure 11

Capacitor (μf)	Output Pulse Width	
	Minimum	Maximum
0.0068	0.99μs	5.1μs
0.0018	3.4μs	13.5μs
0.0047	9μs	35μs
0.012	23μs	90μs
0.033	62μs	248μs
0.082	153μs	615μs
0.22	410μs	1650μs
0.56	1.1ms	4.2ms
1.5	2.8ms	11ms
3.9	7.3ms	29ms
10	19ms	75ms
27	50ms	200ms
400	0.8sec.	2.4sec.

6.5 Crystal Controlled Oscillator

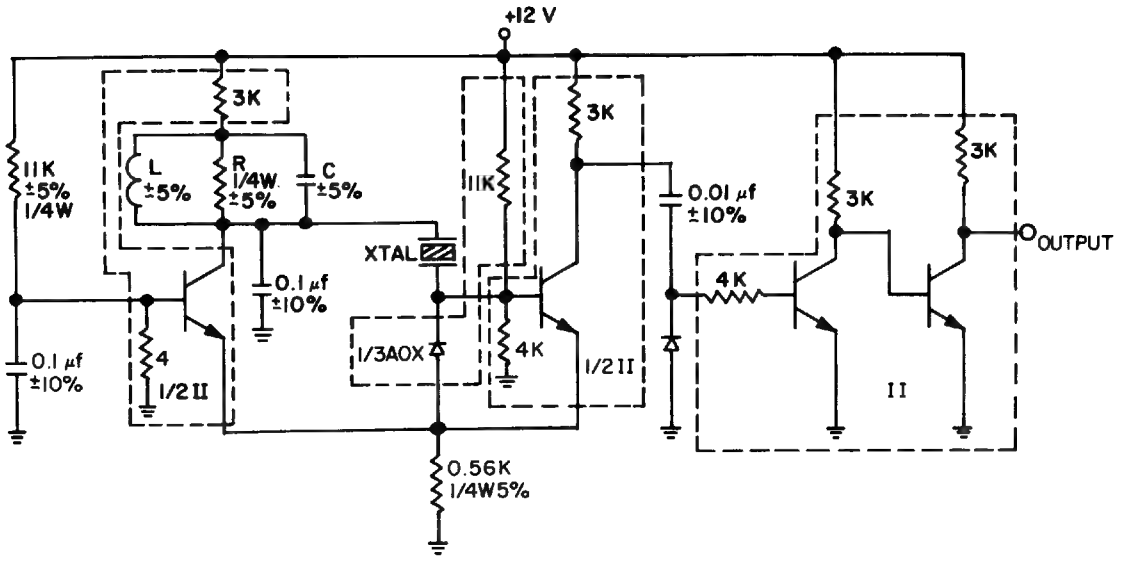


Figure 12

A broad range of frequencies can be obtained from this basic oscillator circuit by varying the values of R, L, C, and by selecting a crystal of the desired frequency. The oscillator is self-starting upon the application of the power supply voltage and generates a rectangular waveform at its output with the fan-out capability of the SLT-700 AI module.

Typical component values and the resultant frequency are shown below:

Frequency	Xtal f	L (µh)	C (µf)	R (KΩ)
100KHz	100KHz	1300	.002	3
128KHz	128KHz	910	.0016	4.7
360KHz	360KHz	175	.0011	9.1
720KHz	720KHz	164	.0003	2.7
1.0MHz	1.0MHz	16	.0016	6.2
1.6MHz	1.6MHz	82	.00012	2.7

6.6 EIA to SLT Converter

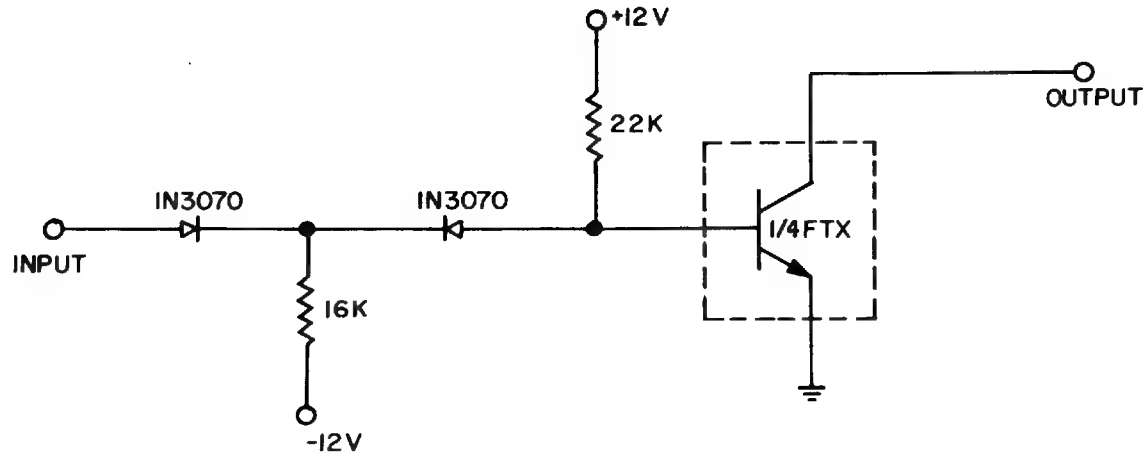


Figure 13

Note: All resistors are 1/4w, 5% unless otherwise specified.

The circuit above is an EIA to SLT Converter. The input voltage levels are given below. The converter drives the standard SLT-700 circuit family modules.

Input Voltage Levels

Up Level:	Max. Voltage	+25 volts
	Min. Voltage	+3.0 volts
Down Level:	Max. Voltage	-3.0 volts
	Min. Voltage	-25 volts

6.7 SLT to EIA Converter

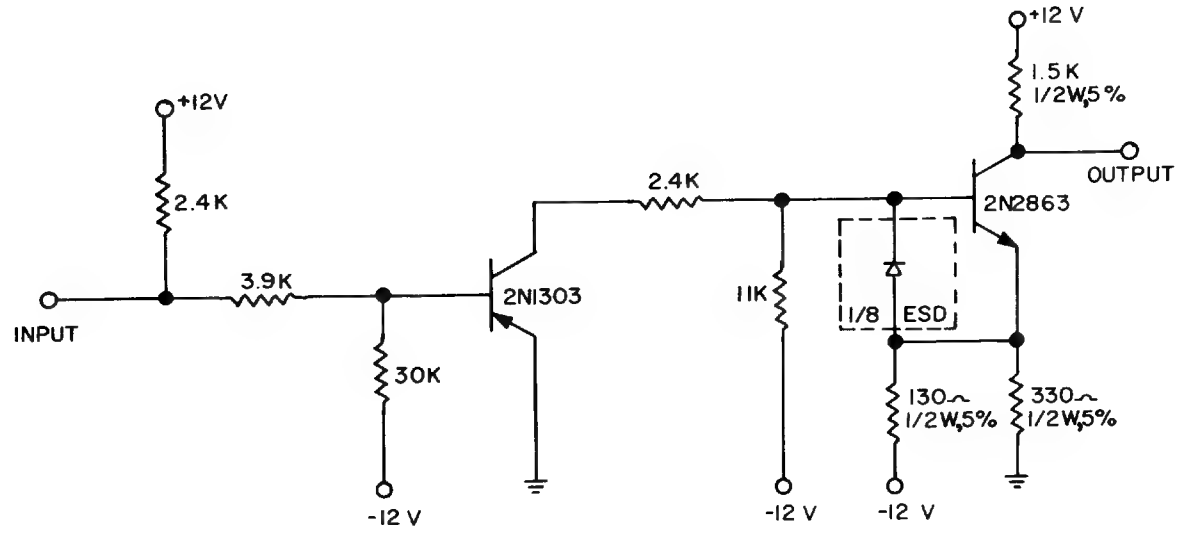


Figure 14

Note: All resistors are 1/4w, 5% unless otherwise specified.

The circuit above is an SLT to EIA Converter. It is driven by the standard SLT-700 circuit family modules. The output voltage levels are given below.

Output Voltage Levels

Up Level:	Max. voltage	+12.9 volts (5 ma.)
	Min. voltage	+ 5.0 volts
Down Level:	Max. voltage	- 5.0 volts
	Min. voltage	- 7.5 volts (5 ma.)

6.8 Indicator Drivers

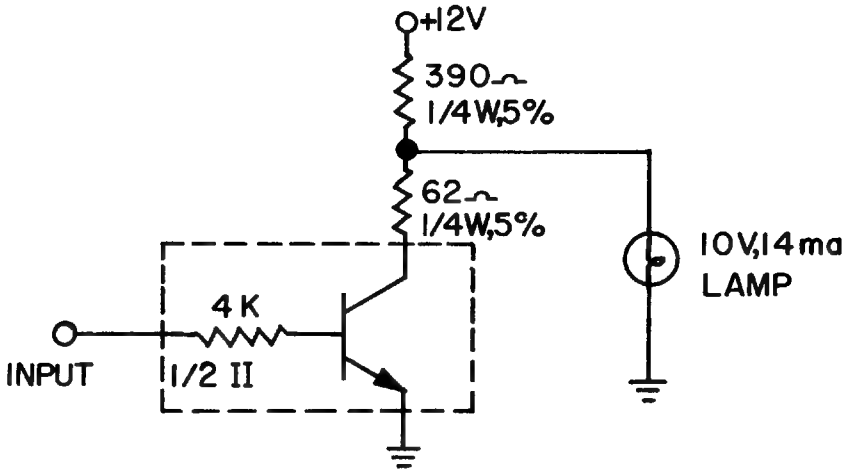


Figure 15

Down-Level Indicator Driver

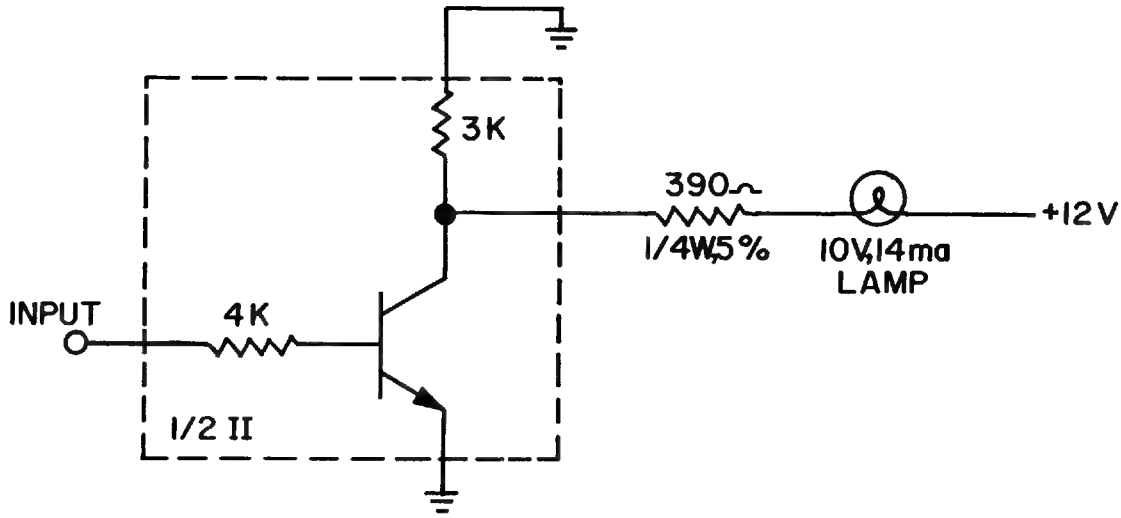


Figure 16

Up-Level Indicator Driver

These indicator circuits are for use where brightness is not essential. They may be driven from any SLT-700 logic block with a collector resistor. The Down-Level Indicator Driver will turn on the lamp when the driving logic block is at its most negative down level (a logical "0"). The Up-Level Indicator driver will turn on the lamp when the driving logic block is at its most positive up level (a logical "1"). A typical lamp cartridge is Dialight Corporation catalog No. 39-10014-1535.

Where greater light intensity is needed the following Up-Level Indicator Driver may be used.

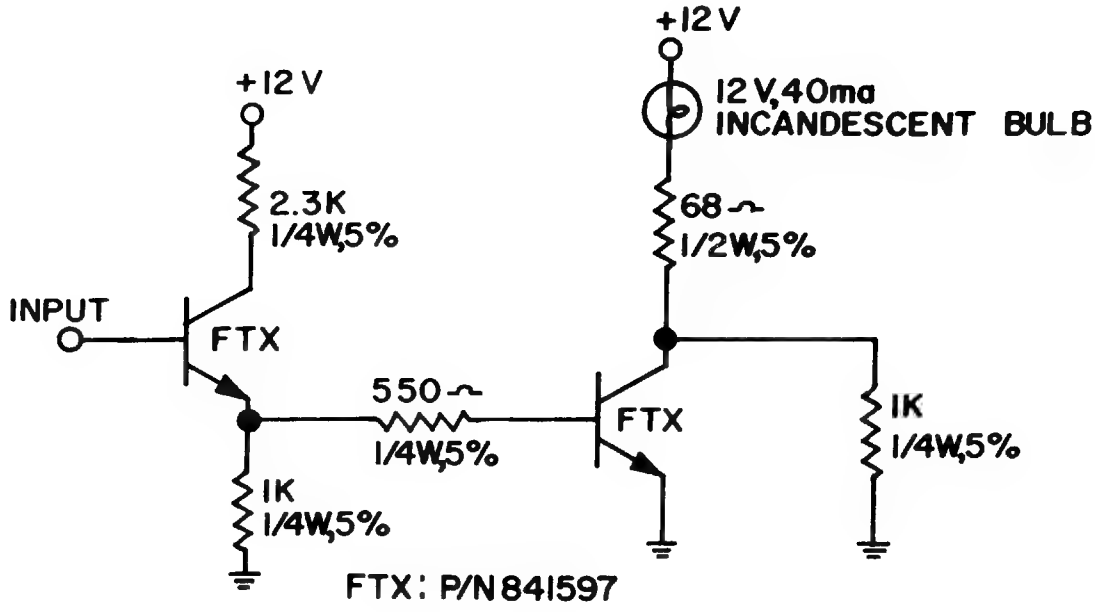


Figure 17: Up-Level Indicator Driver

6.9 Reed Relay Driver

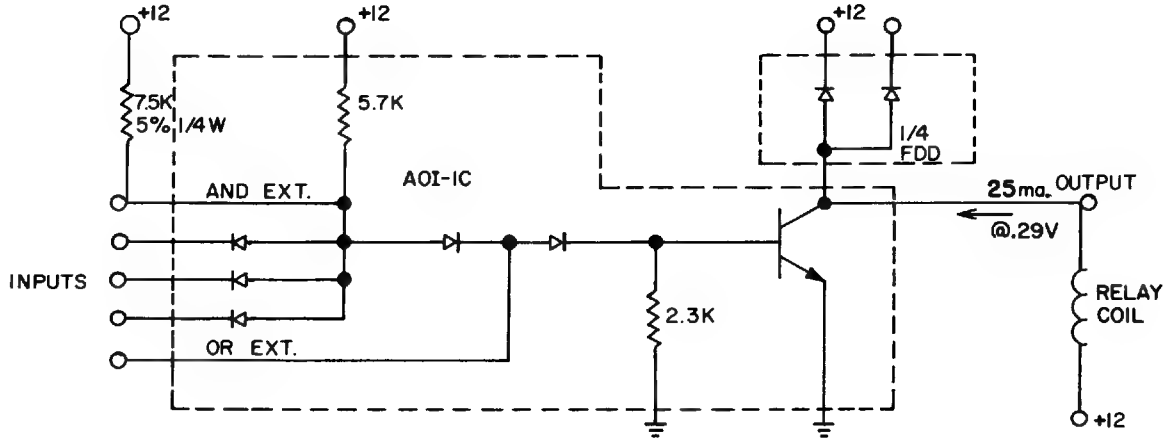


Figure 18

Reed Relay Driver (con't.)

The AND Extend pin may be used in conjuction with an FDD module to provide a maximum fan-in of 10 inputs. Similarly, the OR fan-in can be extended by the use of an AOX module and a discrete 7.5K resister.

The output of the circuit is connected to the inductive load as shown. The maximum allowable drive current is 25ma. @ .29 volts. The FDD module provides suppression to insure that V_{CE} at turn-off does not exceed breakdown.

Reed relays suitable to the above application are available from IBM.

6.10 200 MA. Relay Driver

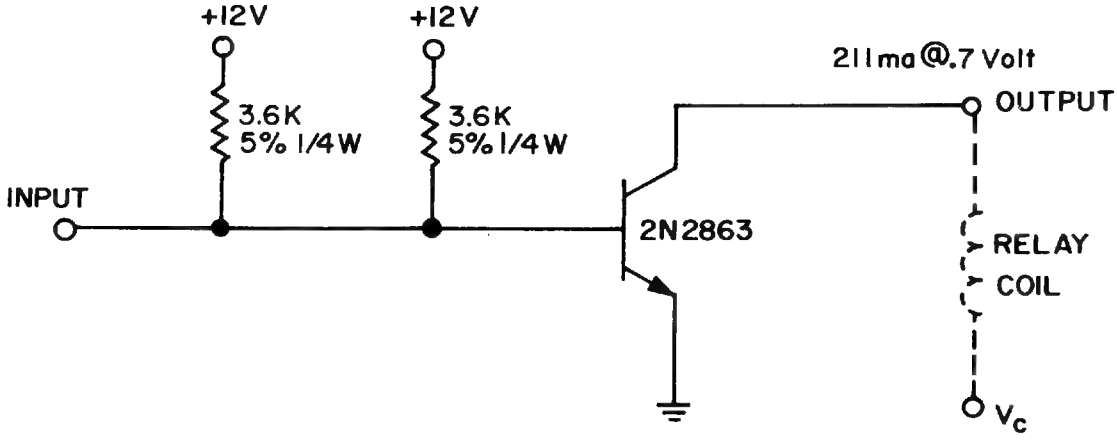


Figure 19

The 200 ma. Relay Driver must be driven by an AOI module (P/N 841592) using 2.9K loads with no further branching.

The output shown in the figure above should be connected to the inductive load. It is understood that suitable suppression be used to insure that V_{CE} at turn-off does not exceed the breakdown voltage of the transistor (25 volts).

The maximum drive current available is 211 ma. @ .7 volts.

6.11 300 Ma. Relay Driver

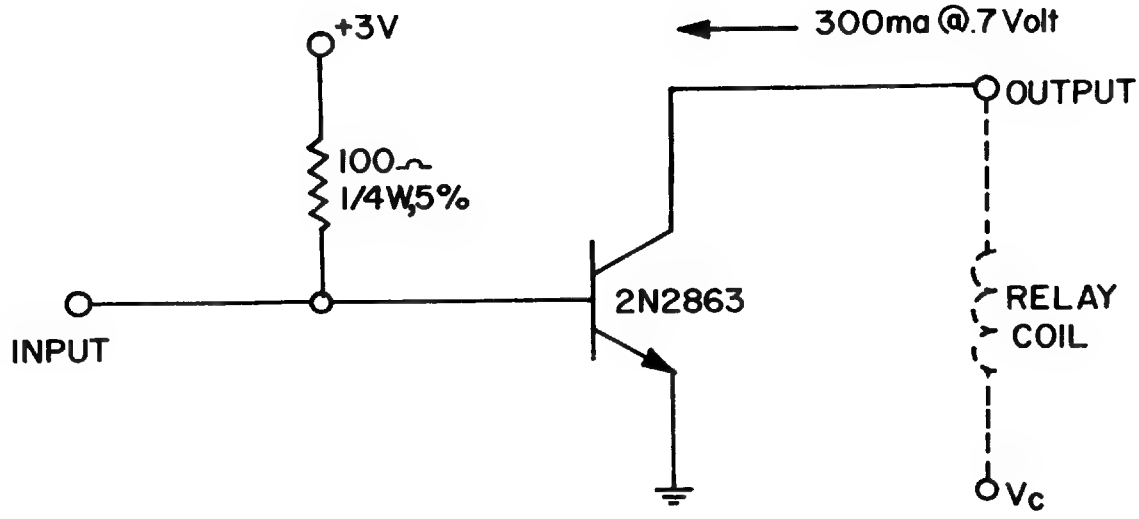


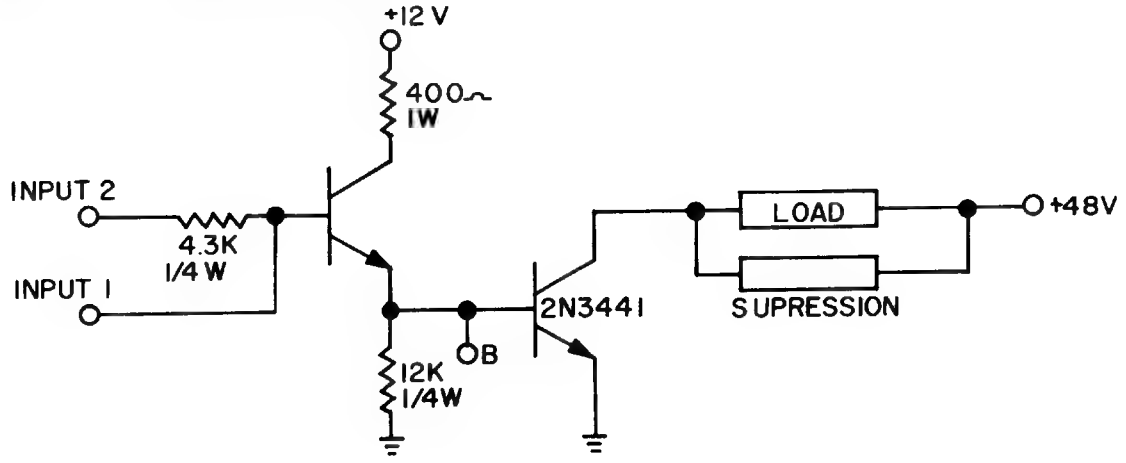
Figure 20

The above relay driver may be driven by an AOI-1C (no load) module.

The inductive load is connected to the output shown above. It is understood that suitable suppression be used to insure that V_{CE} at turn-off does not exceed the breakdown voltage of the transistor (25 volts).

The maximum drive current available is 300 ma.@.7 volts.

6.12 550 ma. Solenoid Driver



The circuit shown in Figure 21 is designed to drive 48V solenoid coils. When input 2 is at +5.5 volts or above (max. allowable 22v) both transistors are saturated and the output can accept up to 550 ma. When the input is down (between 0.0v and +0.29v) both transistors are off and the output current is approximately zero.

Input 1 can be driven from an AOX-3C (P/N 841596) as shown if an AND function is needed. When this is the case, input 2 should be connected to B.

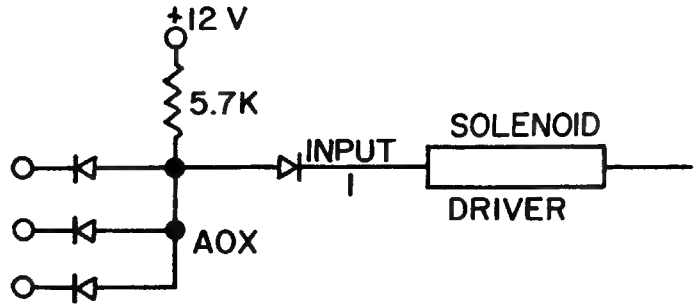


Figure 22

Input 2 can be driven by an AOI-2C (P/N 841593), AOI-1C (P/N - 841592), II-1C (P/N 841594), or any circuit equivalent to the one shown below:

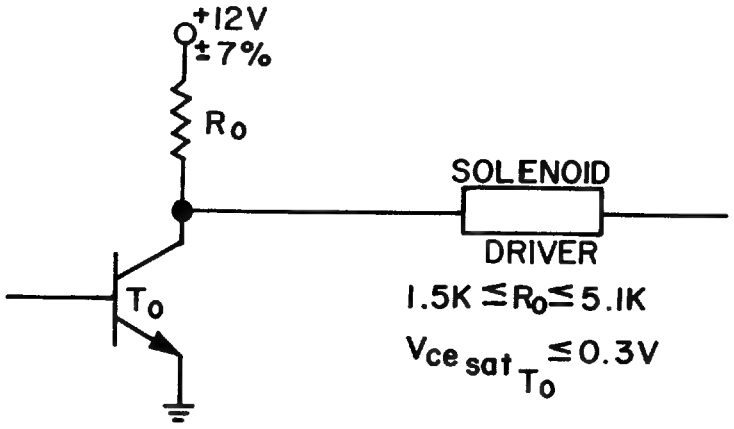


Figure 23

When this is the case, input 1 is not used.

Suitable suppression should be placed around the inductive load to insure that V_{CE} at turn-off does not exceed 140v.

7.1 Signal Hold Circuit

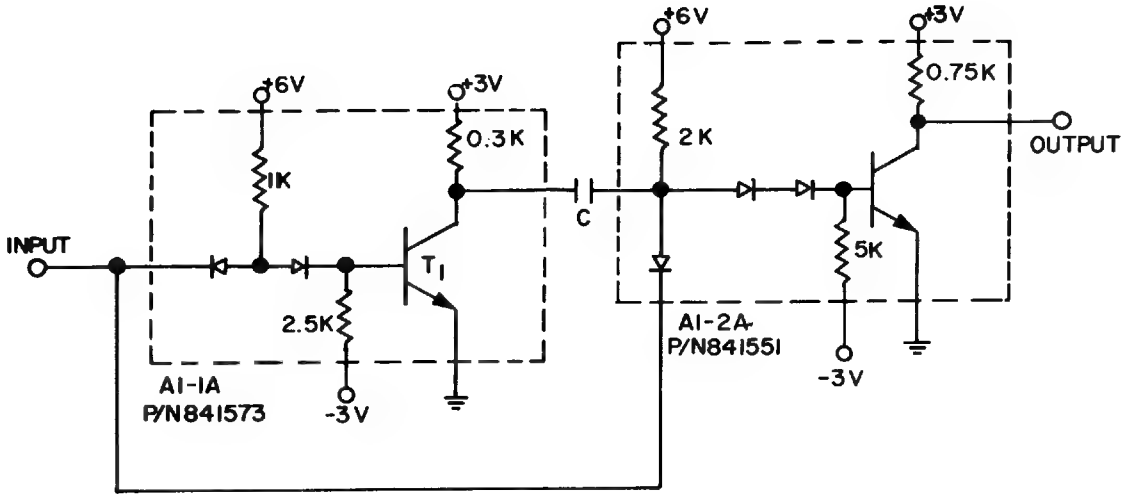
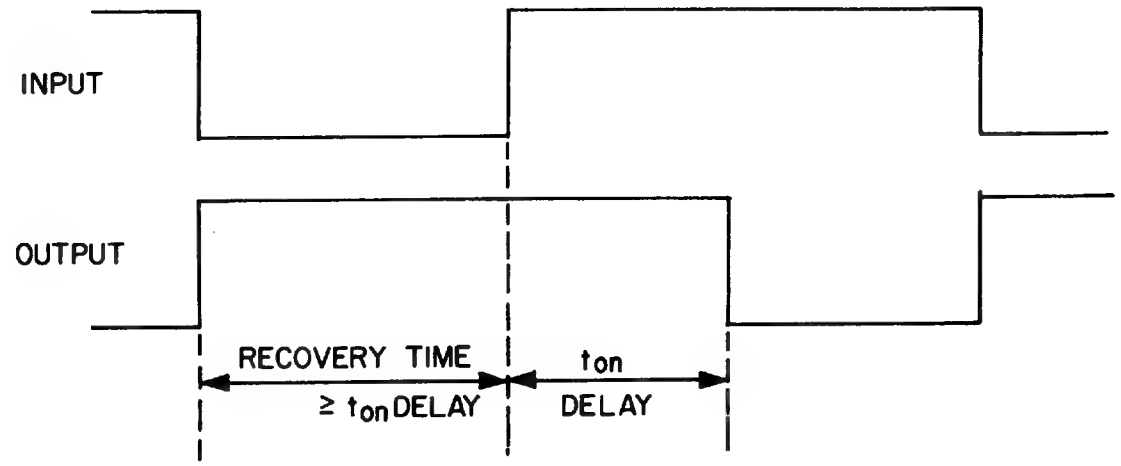


Figure 1



The output signal is inverted and delayed by the T_{on} delay of the circuit. This delay is determined by the capacitor C as, for example:

C (picofarads)	DELAY (nsec.)
150	200
180	250
240	310

Delay Circuit - (225ns & 250ns) .

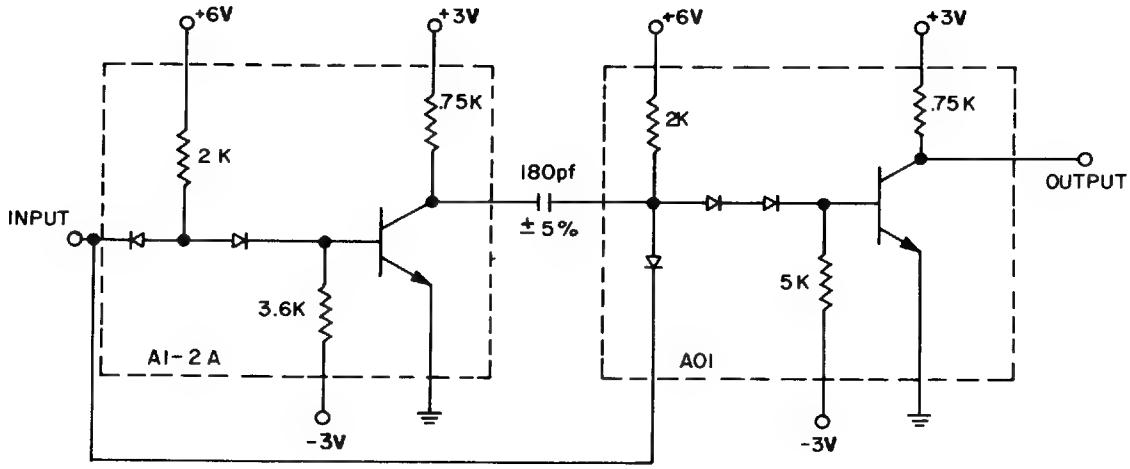


Figure 2

AI-2A(P/N841551): td=225ns
AI-1A(P/N841573): td=250ns

The above delay circuit utilizes an AI-2A and AOI-2A module to give a fixed circuit delay of 225ns.

If the AI-2A is replaced by an AI-1A module, then a fixed circuit delay of 250ns can be obtained.

7.3 Single Shot (Variable)

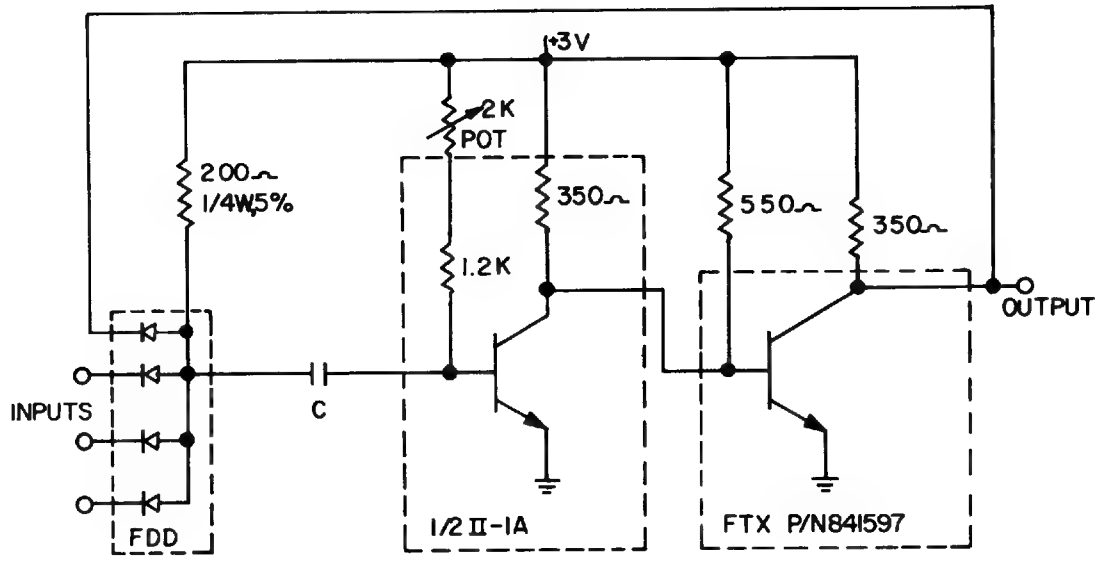
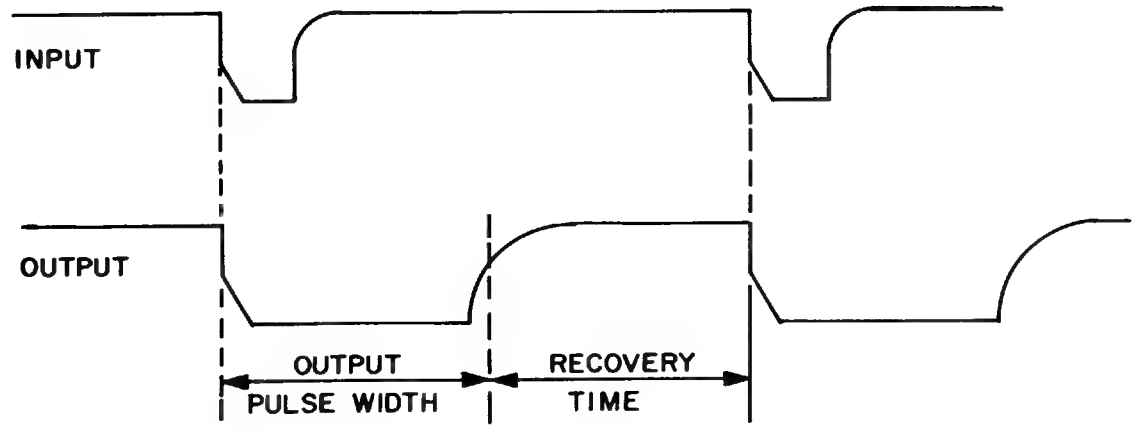


Figure 3



Capacitor C	Output Pulse Width		Minimum Recovery Time
	Minimum	Maximum	
100pf	78ns	207ns	92ns
300pf	234ns	620ns	276ns
0.001μf	780ns	2.07μs	920ns
0.0033μf	2.57μs	6.85μs	3.04μs
0.01μf	7.8μs	20.7μs	9.2μs
0.033μf	25.7μs	68.5μs	30.4μs
0.1μf	78μs	207μs	92μs
0.33μf	257μs	685μs	304μs
1.0μf	780μs	2.07ms	920μs
3.3μf	2.57ms	6.85ms	3.04ms
10μf	7.8ms	20.7ms	9.2ms
27μf	21.0ms	56.0ms	25ms

The single-shot is triggered by a negative-going pulse , having a transition no greater than 50 nanoseconds (ns) and a width no less than 30ns. Upon triggering, the output drops to the saturation level for the pre-set duration before returning to the +3v level. A minimum recovery time for the capacitor is required before the next trigger pulse can be applied. The output pulse width will be of incorrect duration if the single-shot is triggered during the recovery period.

7.4 Crystal Oscillator

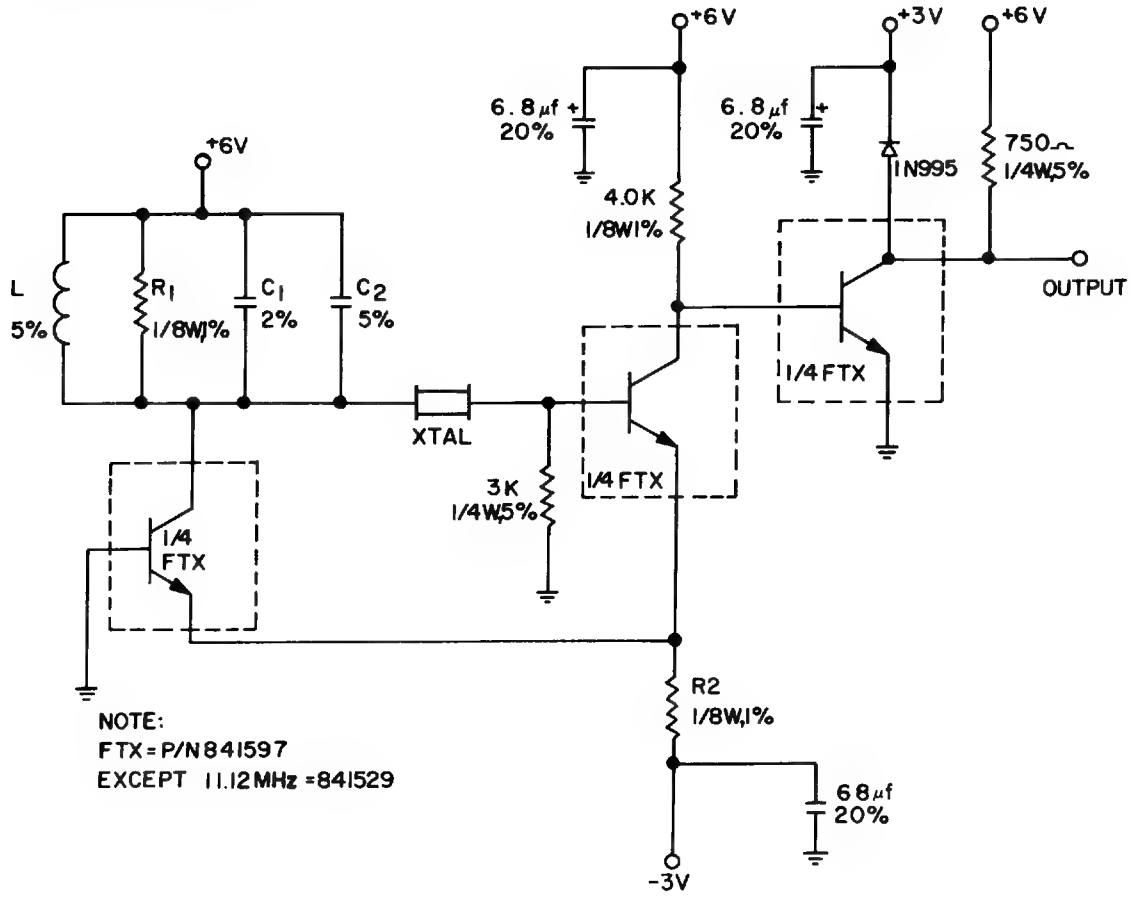


Figure 4

The free-running crystal oscillator serves as a pulse generator. It produces pulses or voltage variations of a definite frequency which are determined by values of L, R_1, R_2, C, and the crystal used.

The circuit consists of a basic switching circuit whose frequency is determined by the quartz crystal. The crystal vibrates and develops a sinusoidal voltage that is amplified and clipped to produce the square wave output. The tank circuit provides regenerative feedback to sustain the crystal oscillation.

Crystal Oscillator (con't.)

Typical component values and the resultant frequencies are shown below.

Frequency	FTX P/N	Crystal	R_1 (Ω)	R_2 (Ω)	C_1 (pf)	C_2 (pf)	L (μh)
1.44MHz	841597	1.44MHz	340	698	750	5.1	15
11.12MHz	841529	11.12MHz	301	698	120	5.0	16

If the parallel combination of C and C_2 is replaced by a single capacitor C, then the following oscillator frequencies are available.

Frequency	FTX P/N	Crystal	R_1 (Ω)	R_2 (Ω)	C	L (μh)
2.4MHz	841597	2.4MHz	147	715	0.0011 μf(2%)	3.9
3.2MHz	841597	3.2MHz	382	698	390pf(1%)	6.2

The frequencies given above are typical values. They, by no means, exhaust the number of frequencies available.

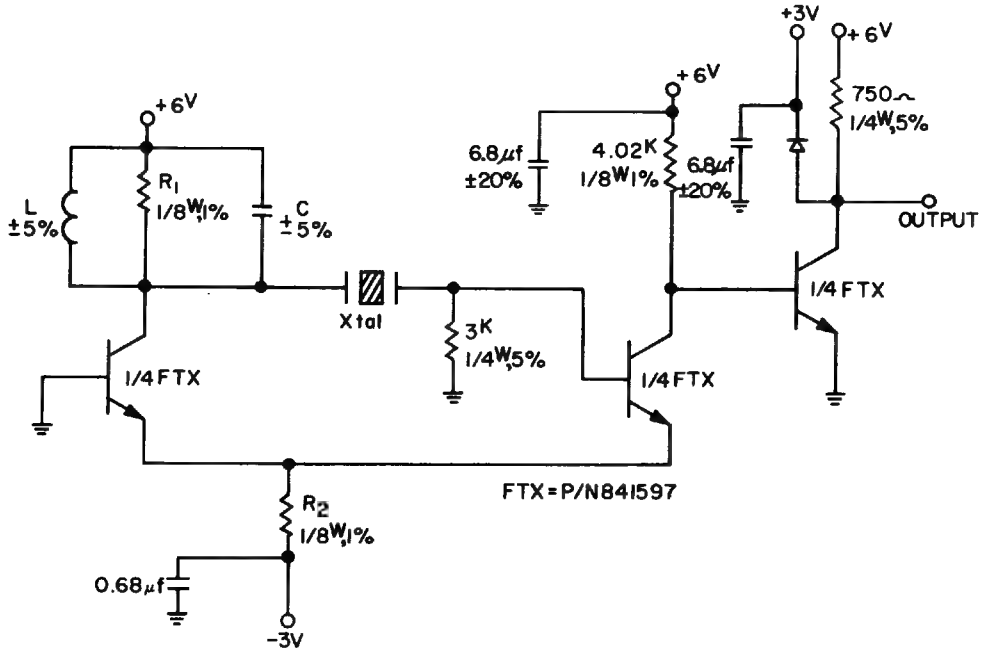


Figure 5 Crystal Controlled Oscillator

This basic free-running crystal controlled oscillator circuit will generate pulses, with the drive capability equal to a standard SLT-30 AI module, over a broad range of frequencies by varying the values of L, C, and R used.

A sampling of component values and the resultant frequency are:

Frequency	FTX P/N	Crystal	R_1 (Ω)	R_2 (Ω)	L (μh)	C (pf)
4MHz	841597	4MHz	511	787	8.2	192
5MHz	841597	5MHz	681	768	8.2	12

7.5 EIA To SLT Converter

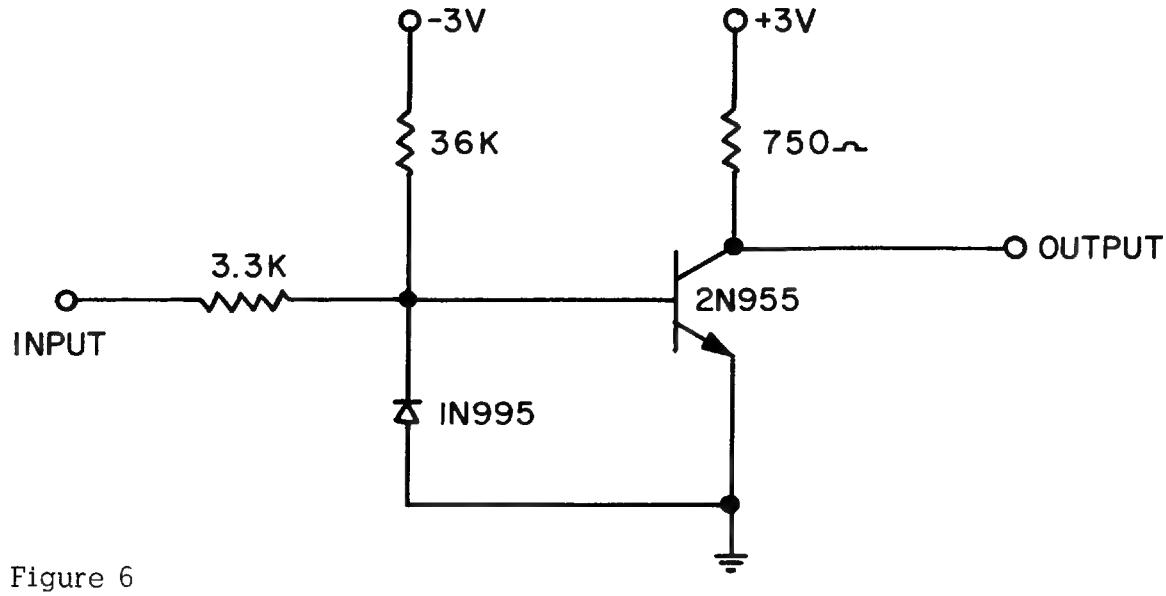


Figure 6

The above circuit is an EIA to SLT converter. It is driven by any circuit that meets the EIA specifications. The output of the circuit provides the standard SLT (30ns family) voltage levels.

Note: All resistors are 1/4w, 5% unless otherwise specified.

7.6 SLT To EIA Converter

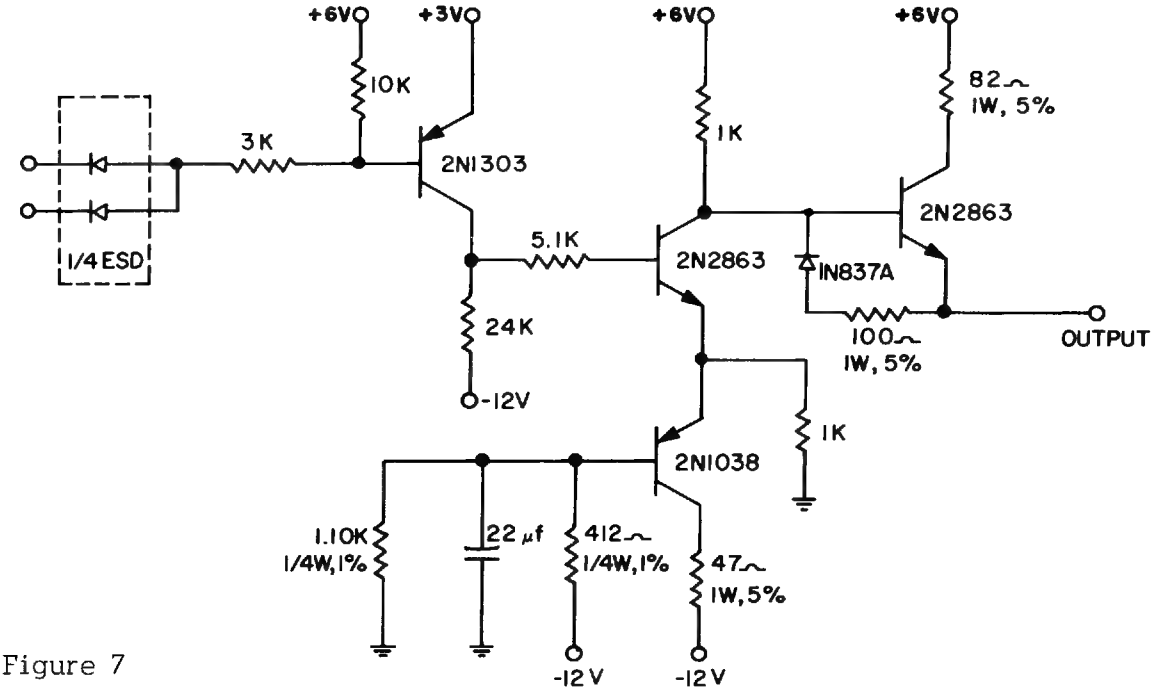


Figure 7

The circuit shown in figure 33 will convert an input signal voltage of 0 to +3 volts to an output signal voltage of +5 to -5 volts. This circuit will drive any circuit that meets the EIA specifications.

Note: All resistors are 1/4w, 5% unless otherwise specified.

7.7 Transmission Line Driver And Terminator

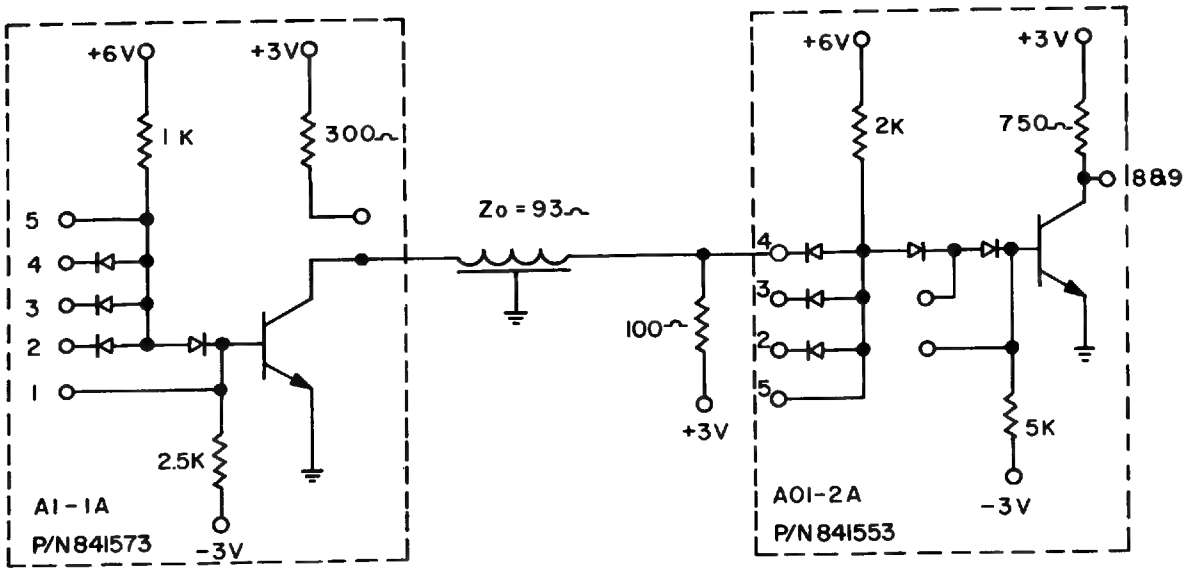


Figure 8

The AI-1A module may be used to drive a transmission line as shown in Figure 8. The AI module consists of a diode positive AND circuit followed by a saturating transistor inverter. Note that the AI collector resistor is not used.

The characteristic impedance of the transmission line is 93Ω . To match the impedance of the transmission line, a 100 resistor is used in conjunction with an AOI module. Thus, the terminating resistor with the ON impedance of the AOI matches the characteristic impedance of the transmission line which can be coaxial cable, flat-cable or printed wire.

If a greater fan-out is desired, the AOI module on the receiving end may be replaced by an LA module. A total of 5 LA modules can be branched off at the receiving end providing that each module is less than 6 inches from the terminating network. It is important to note that only one AOI module is allowed if the LA module is not used.

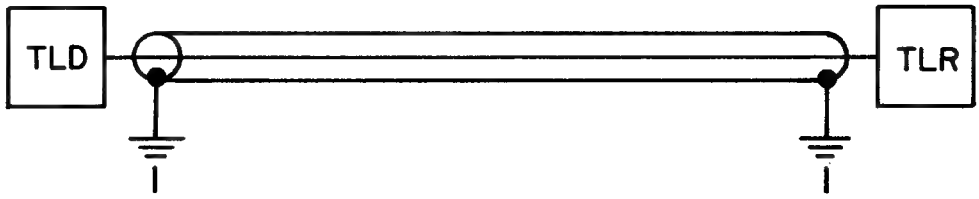
A typical application is to use a programmable delay line ($Z_o = 93\Omega$) so that the output pulse width is the same as the input pulse width, but is delayed for a selected time interval. A typical programmable delay line would offer delays of 5-500ns in 5ns increments.

Transmission Line Driver And Terminator (con't.)

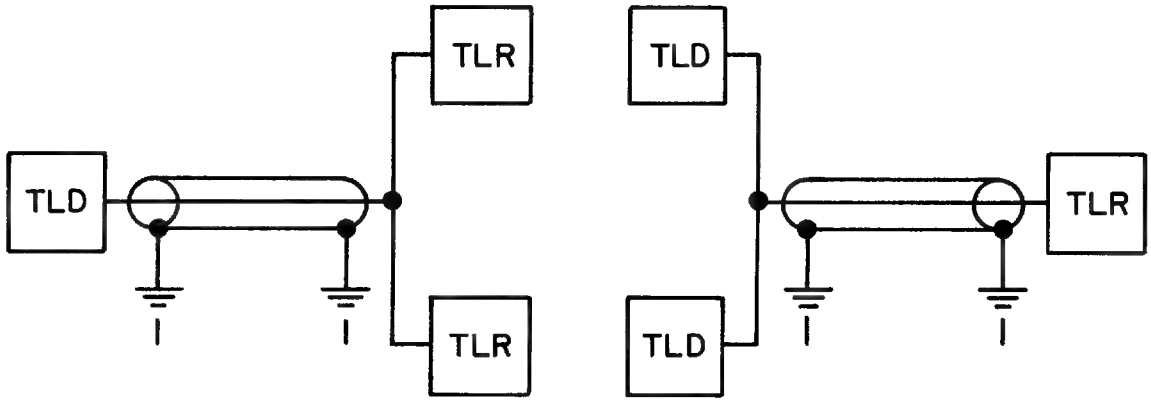
The previous remarks also apply to the 700ns family. For 700ns family operation, each 30ns family module is replaced by its corresponding module in the 700ns family.

If a fan-out to several logic modules is desired from a single Transmission Line Receiver, then the TLR module can be used.

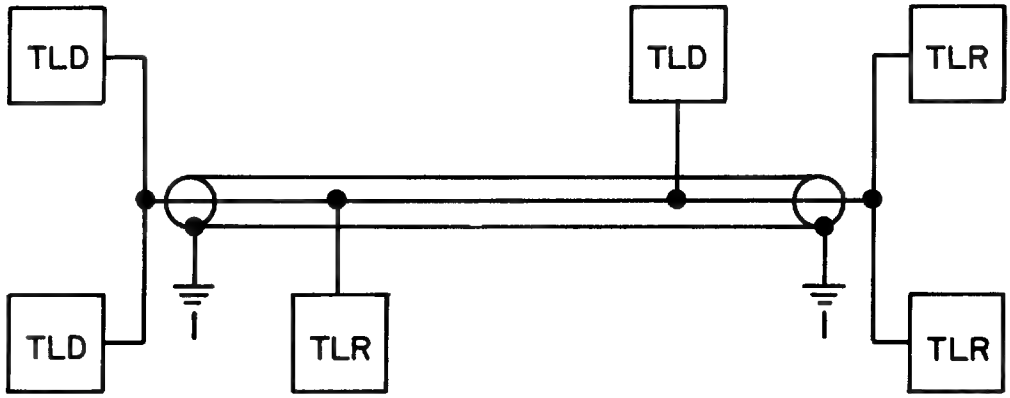
There are several combinations and applications of Transmission Line Drivers (TLD) and Transmission Line Receivers (TLR); some of these combinations are shown below.



Simplex



Distributive Simplex



Multiplex

7.8 Switch and Contact Inputs

Some care must be exercised in controlling logic circuits from switch or contact inputs. Two aspects require particular attention. First, for many switches contact bounce is not specified. Bounce sensitive applications may require an integrating circuit or device such as pulse-shaping circuits or a latch interface. Second, the contact material and its operating environment may necessitate high contact currents or voltages to insure an adequate contact closure. In applications where the product of the open circuit voltage and the closed circuit current is greater than 0.4 VA, conventional switches with silver contacts may be used with reasonable assurance of contact closure. For low voltage use, where open circuit voltage is between 5 and 20 volts DC, the product of volts times amperes should probably exceed 0.8 VA.

Gold plated contacts in contamination-free environments, such as in IBM Reed Relays, may be used with no minimum VA requirements, and generally, should not be used where open circuit voltage is more than 15 volts.

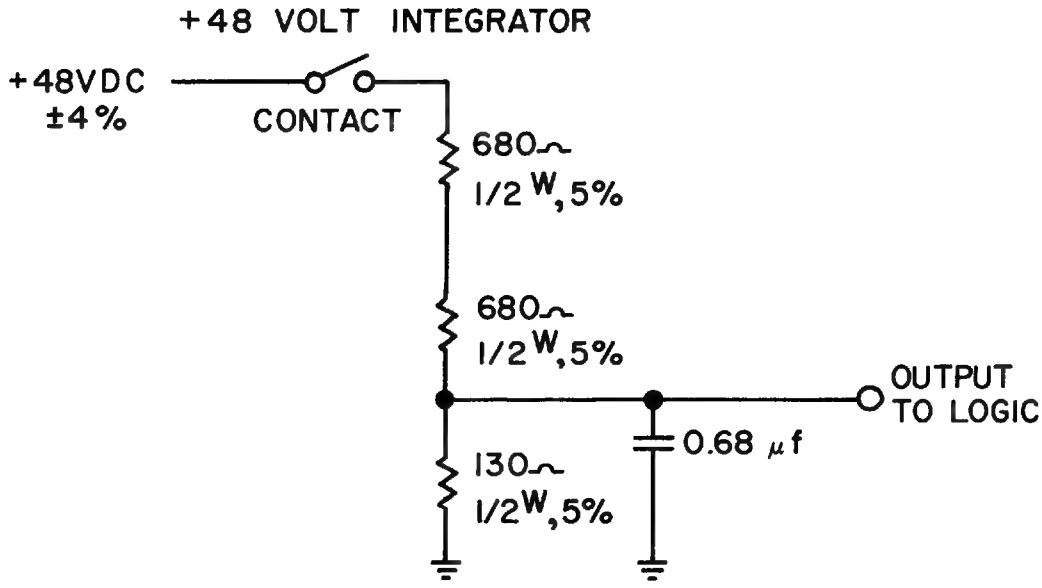


Figure 9

This is a typical circuit for use with either the SLT 30 or SLT 700 families. The circuit interfaces between silver contacts of a conventional switch and one logic input (AI or AOI). The value of the delay capacitor shown should be adjusted to compensate for the bounce characteristics of the contact.

Switch and Contact Inputs (con't.)

An improvement in the integrater wave shape and further isolation may be obtained by inserting a transistor stage between the switch and the logic circuits as shown in Figure 10 for the SLT-700 family.

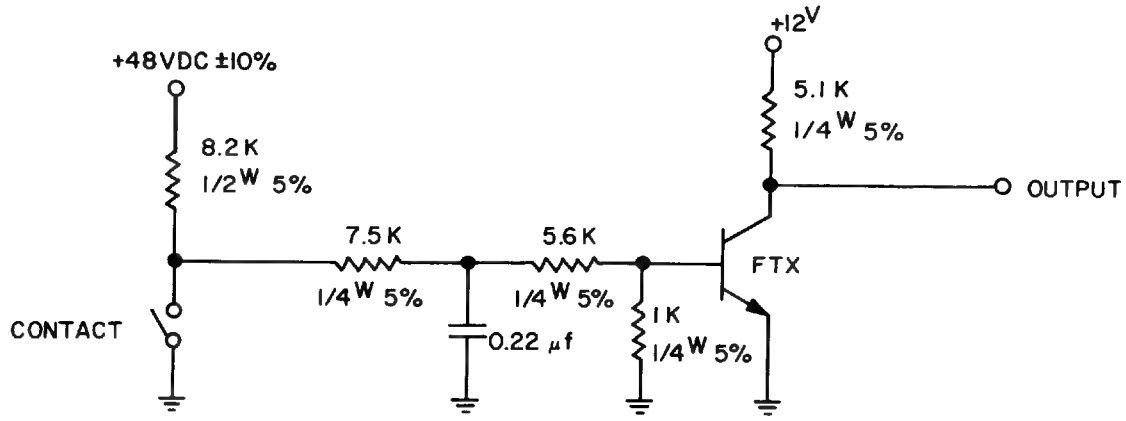


Figure 10

The output drive capabilities are the same as the SLT 700 AI block. As before, the value of the capacitor should be chosen to eliminate bounce.

7.9 Indicator Drivers

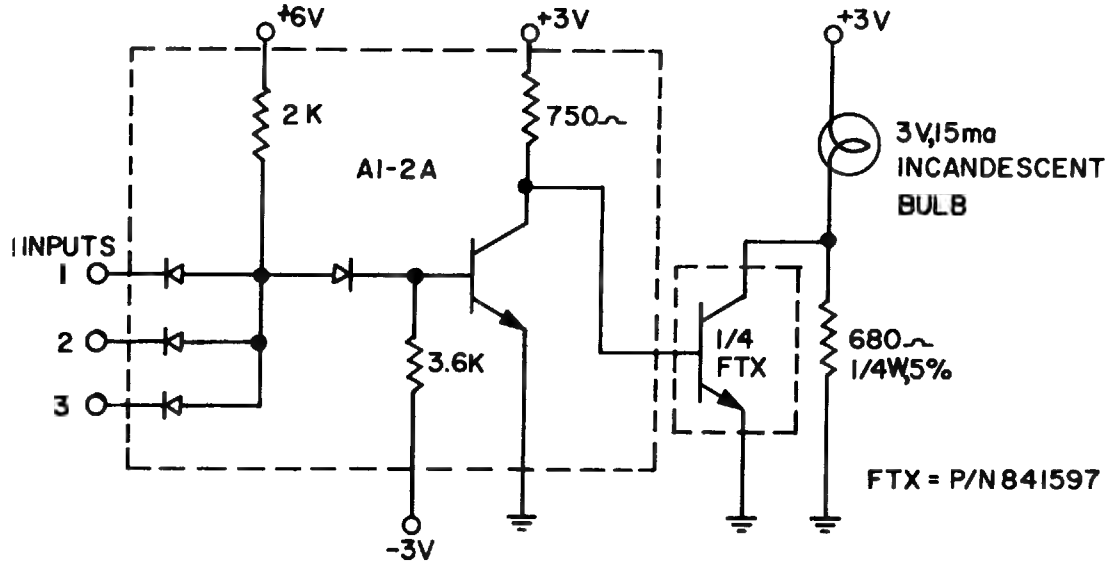


Figure 11: Down-Level Indicator Driver

Indicator Drivers (con't.)

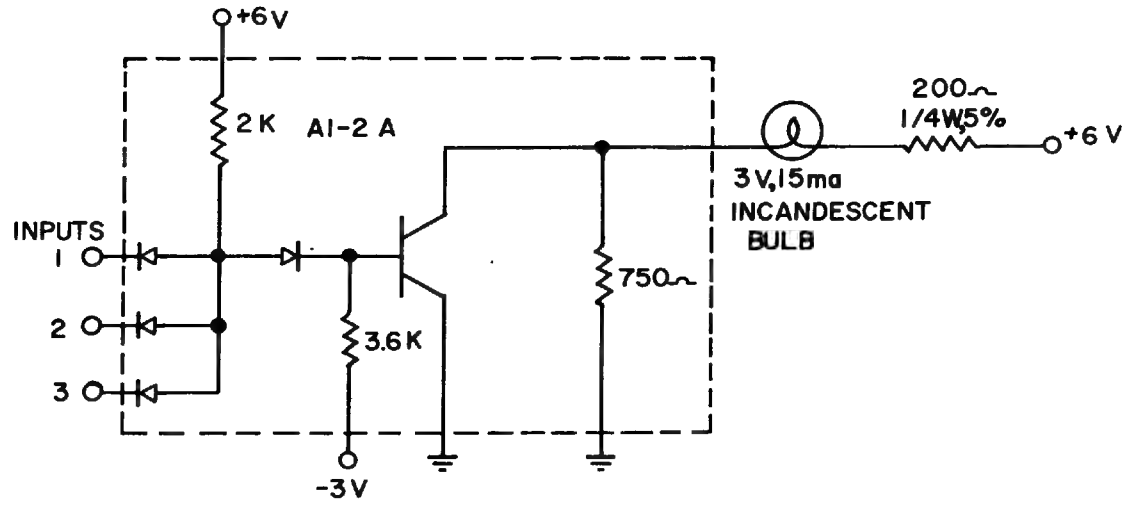


Figure 12 Up-Level Indicator Driver

These indicator circuits are for use where brightness is not essential and where multiple inputs must control the indicator. Inputs may be driven from any SLT - 30 logic block. Loading is the same as the AI.

The Down-Level Indicator Driver will turn on the lamp when any one (or more) of its three inputs is at a logical "0", that is, then the logic block driving any input is at its most negative down level. The Up-Level Indicator Driver will turn on the lamp when all of its inputs are at a logical "1", that is, when all logic blocks driving inputs are at their most positive up level. In both Drivers, if an input is not used it may be left disconnected.

If the logic function provided by the drivers in Figures 11 and 12 is not required, the Up-Level Indicator Driver shown in Figures 13 and 14 may be used. One of these Indicator Drivers may be driven from an SLT-30 logic block with collector resistor in addition to normal diode loads.

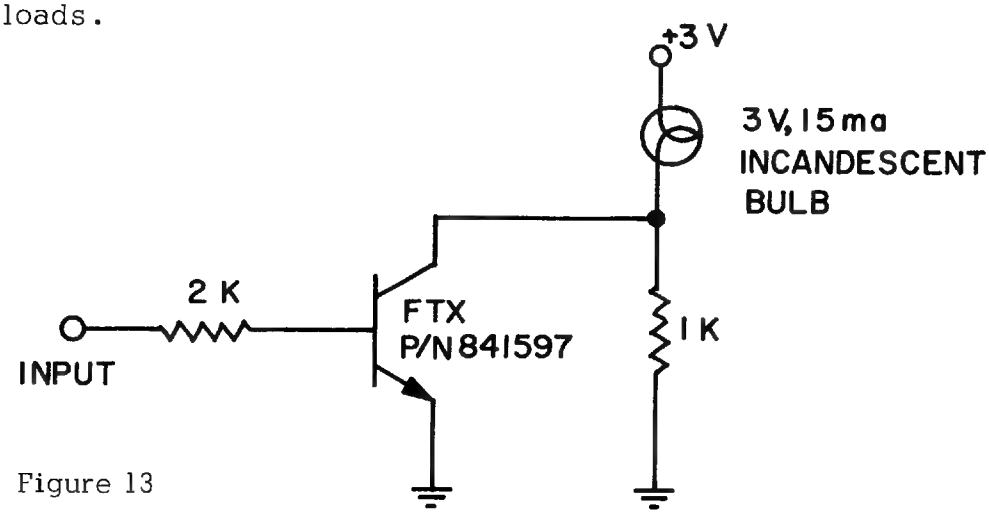


Figure 13

If greater brightness is needed the following Up-Level Indicator may be used:

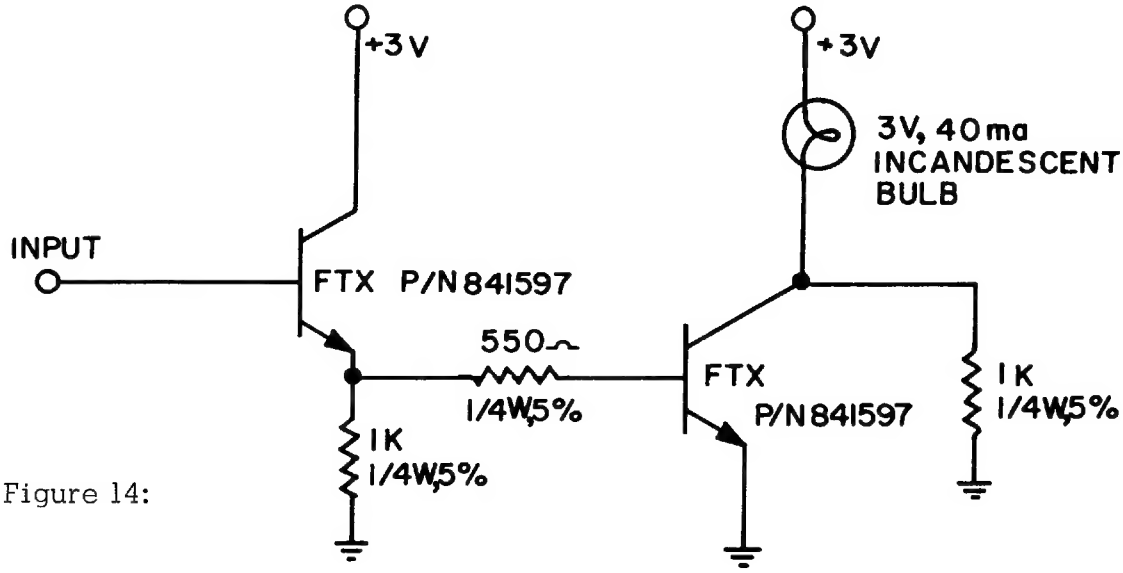


Figure 14:

7.10 Reed Relay Driver

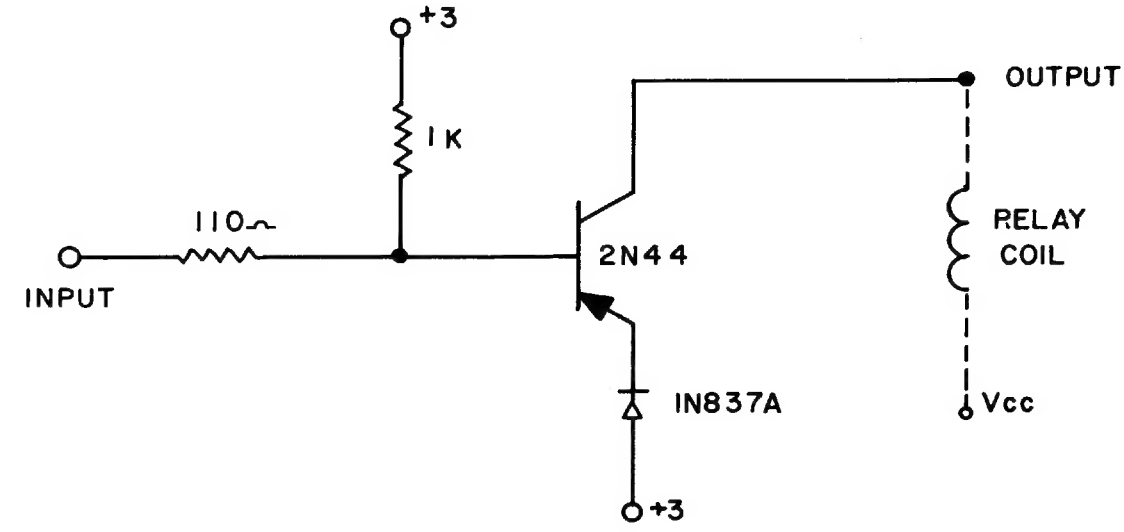


Figure 15

Note: All resistors are 1/4w, 5% unless otherwise specified.

The input is driven by an AI module. No further branching on the AI module is permitted.

The output is connected to the inductive load and power supply as illustrated. Suitable suppression should be used to prevent V_{ce} at turn-off from exceeding the breakdown voltage of the transistor (45 volts).

Reed relays suited to the above application are available from IBM.

Maximum relay coil current should not exceed 120 ma D. C.

7.11 450 Ma. Relay Driver

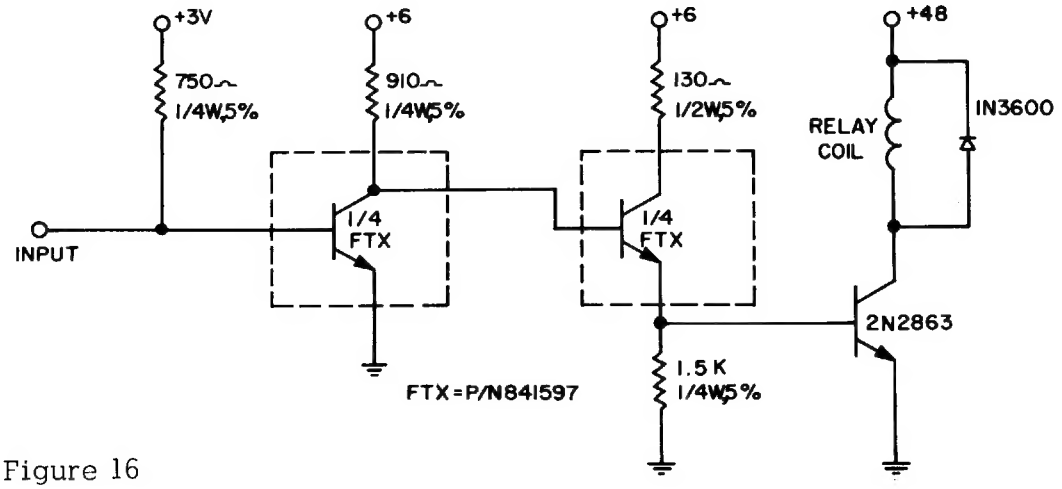


Figure 16

The inductive load is connected to the collector of the 2N2863 transistor as shown above. The diode provides the suppression needed to insure that V_{ce} at turn-off does not exceed the breakdown voltage of the transistor which is 65 volts.

The input of the relay driver may be driven by an AI or AOI module with no further branching on the module allowed.

7.12 2 Second Timer

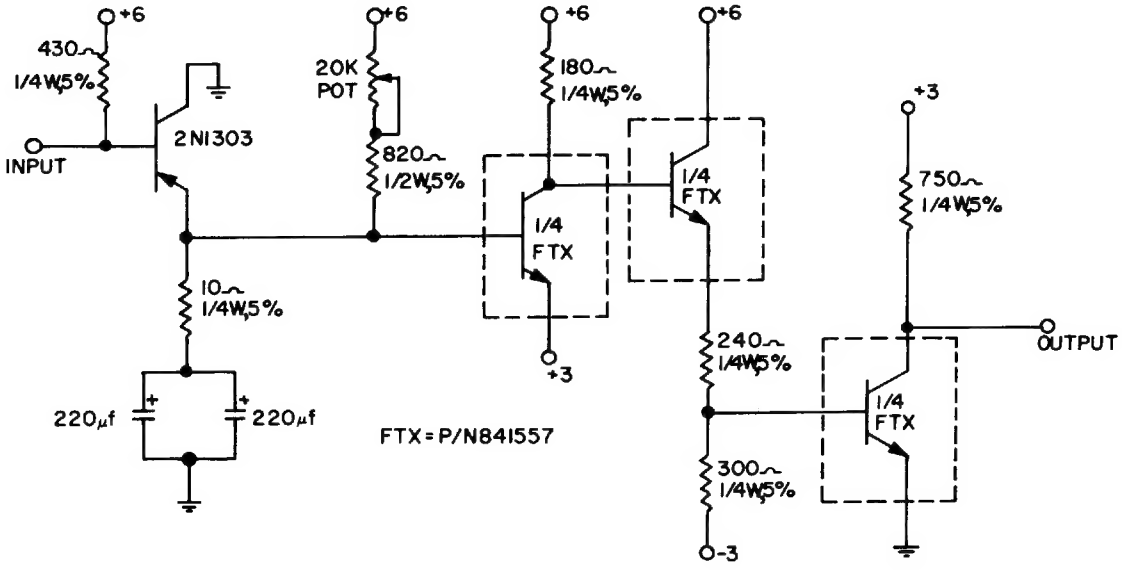


Figure 17

The two second timer as shown in Figure 17 can be driven by an AI, or AOI module providing that the collector resistor of the module is not used.

The 20K potentiometer provides adjustment for the timer.

7.13 Variable Time Delay, .1 to 2 Sec.

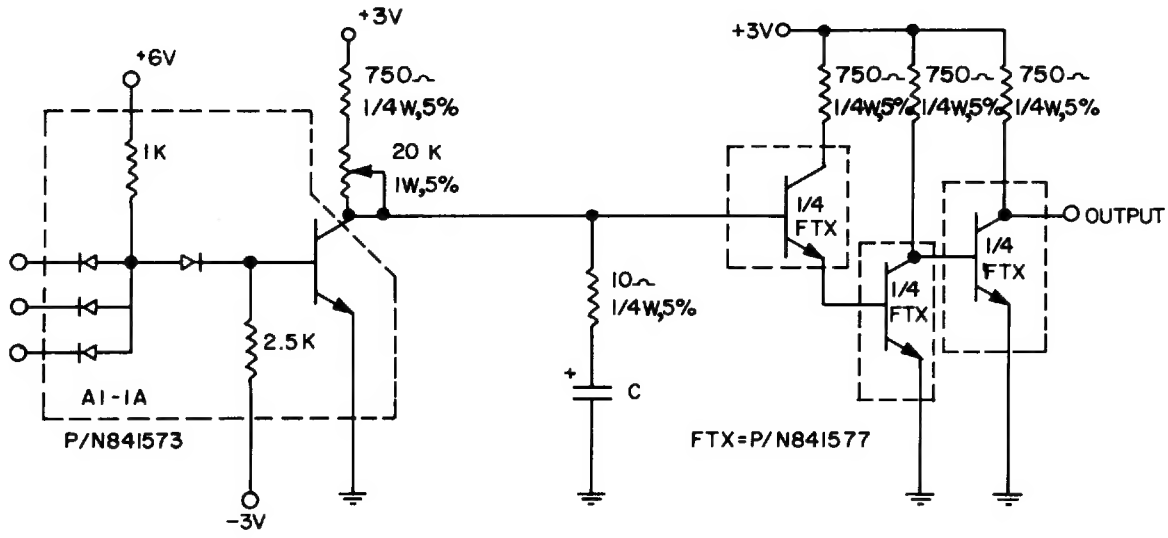


Figure 18

The input circuit of the variable time delay circuit is an AI module.

The following table illustrates the adjustable delay ranges available.

Adjustable Delay Range, Sec.	Capacitance, pf
0.09 to 0.82	120
0.52 to 1.60	240
0.80 to 2.45	360

The delay is adjusted by means of the 20k potentiometer.

8.0 Mixing Families-Rules

The two SLT families can be intermixed in accordance with the following restrictions or loading adjustments.

	700	30
700	No restrictions	Only AI & AOI
30	Only AOI & AI	No restrictions

Example:

A 30 nsec. AOI module (P/N 841553) driving 700 nsec. AOI modules (P/N 841593).

Available collector current 30 nsec AOI (P/N 841553) = 22.5 ma

$K_1 = I_{in}$ of 700 nsec AOI (P/N 841593) ($@V_{in}$ =o.30 V) = 1.15 ma

I_R of 30 nsec. AOI (750Ω Collector Resistor) = 4 ma

$$I_C - I_R = K_1 N_1 + K_2 N_2 + K_3 N_3 + \cdots\cdots$$

$(22.5 - 4.0)$ ma $= 1.15\ N_1$

Where N_1 = Number of 700 nsec. AOI Loads

Then

$$N_1 = \frac{18.5}{1.15} = 16$$

Therefore in this example an AOI 30 nsec. module can drive sixteen 700 nsec AOI module.